

QFN Style Solder-Down Computer On Module

- 27mm square
- 2.6mm total height
- QS family pin-compatible
- Solder-down version
- QFN type lead style
 - 1mm pitch
 - 100 pads
 - Thermal pad
- Visual solder joint inspection possible after soldering
- Single-sided assembly
- 3.3V power supply



Key Features

- STM32MP235 Dual ARM® Cortex®-A35, 1.2 GHz
ARM® Cortex®-M33, 400 MHz
Vivante® NPU, 0.6 TOPS
- RAM 1GB LPDDR4
- ROM 4 GB eMMC
- Grade Industrial
- Temperature -40°C to 85°C
- Display support
 - LVDS Display Interface
 - 3D GPU: OpenGL® ES 3.1 - Vulkan 1.1, OpenCL™ 1.2, OpenVX™ 1.1, Up to 66 Mtriangle/s, 400 Mpixel/s
 - VPU: H264/VP8 up to FHD (1920×1080)@60 fps
- Connectivity
 - 2x USB 2.0
 - 2x Gb Ethernet, RGMII
 - 1x eMMC/SD
 - 2x CAN-FD
 - 3x UART, 3x I²C, 1x SPI, PWM, SAI
 - Up to 60x 3.3V General Purpose I/O
 - MIPI-CSI (2-lane)

OS Support

- Linux

**Dual
Cortex®-A35
STM32MP2**



STM32MP235

System

Power Supply Regulators
Crystal & Internal oscillators
Cyclic Redundancy Check (CRC)
Watchdogs (I & W)
96-bit unique ID
Up to 176 GPIOs

Security

RIF: Isolation and safe sharing of system resources
Octal SPI OTF Decryption
DRAM OTF Encryption/Dec.
DES, TDES, AES-256 with SCA
SHA-256/512, SHA-3, HMAC
PKA ECC/RSA with SCA
16x Tamper pins
T°, V, F and 32KHz detection
Secure RTC
Analog true RNG

Dual Cortex-A35

Core 1 L1 32kB I / 32kB D	Core 2 L1 32kB I / 32kB D
NEON SIMD MPE	NEON SIMD MPE
512kB L2 cache	
TrustZone	

Cortex-M33 @ 400MHz

16 kB I-Cache	16 kB D-Cache
FPU / MPU / NVIC	TrustZone

LPDDR4 @ 1.2GHz

Shared RAM 640kB including 128kB Retention RAM
Backup RAM 8kB / Boot ROM 128kB / OTP fuse 12kb

Control

3x 16-bit motor control PWM synchronized AC timer	
10x 16-bit timer	5x 16-bit LP timer
4x 32-bit timer	

Multimedia / AI

3D GPU: OpenGL ES3.1 / Vulkan 1.1 / OpenCL 1.2	
AI / NN HW Acceleration: up to 0.6 TOPS	
1080p60 H.264, VP8 Video Decoder	
24b RGB Disp. 1080p @ 60fps	LVDS Display 4 lanes with PHY
DSI Display 4 lanes with PHY	Camera I/F MIPI CSI-2, 2 lanes
Lite-ISP (Camera Pipeline)	Camera I/F 16-bit Parallel

Connectivity

1Gbps ETH/TSN port	1Gbps ETH/TSN port
2x CAN-FD / TTCAN	2x USB2.0 Host HS + HS PHY
3x SDIO3.0 / SD 3 / eMMC 5.1	
16-bit SLC NAND, 8-bit-ECC	
2x Octal SPI, 8x SPI	
5x UART, 4x USART	4x I²C, 4x I3C, 3x I³S

Audio

SPDIF Rx 4 inputs
4x SAI
MDF 8 channels / 8 filters

Analog

3x 12-bit ADC 5 MSPS
Temperature sensor

QS93 | QSMP-23 | QSMP-25 | Differentiating Features

	QS93 i.MX 9352	QSMP-23 STM32MP235	QSMP-25 STM32MP255
Primary Arm® Core	2x Cortex®-A55 1.5 GHz	2x Cortex®-A35 1.2 GHz	2x Cortex®-A35 1.5 GHz
Secondary Arm® Core	Cortex-M33 250 MHz	Cortex-M33 400 MHz	Cortex-M33 400 MHz
RAM	1GB LPDDR4	1GB LPDDR4	1GB LPDDR4
ROM	4 GB eMMC	4 GB eMMC	4 GB eMMC
GPU	2D GFX	66 MTrg/s 400 MPix/s 12.8 GFlops	133 MTrg/s 800 MPix/s 25.6 GFlops
AI/ML/DSP	0.5 TOPS	0.6 TOPS	1.2 TOPS
VPU	-	Decode	De-/Encode
Connectivity	USB 2.0	USB 2.0	USB 2.0, USB 3.0 or PCIe
QS Size	100 pins 27mm square	100 pins 27mm square	108 pins 29mm square
Grade / Temperature	Industrial -40°C to 85°C	Industrial -40°C to 85°C	Industrial -40°C to 85°C

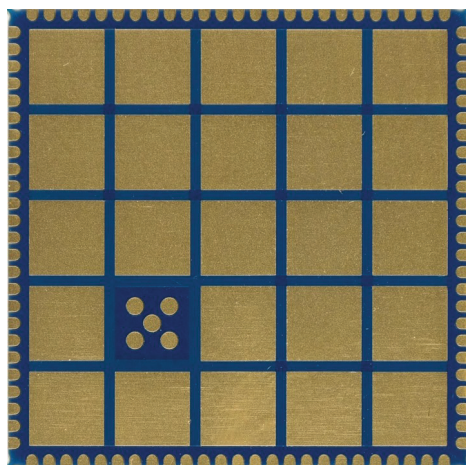
QFN Style Computer On Module Advantages

Defined Return Path

The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller formfactors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation may occur on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

When a module or component is used in a design, the supplier specifies the basis for such a layout. It's not only the pinout which should lead to an easy wiring without the need for crossings. He also has to provide a proper solution for the signal path back to the module. If this return path, mostly the ground plane, cannot be connected near the signal pin, the return current has to take another way and this may result in a loop area. The larger the area, the more radiation and EMI problems may occur.

Ka-Ro QSCOM modules uses a large ground pad on the bottom side. With this a defined ground plane connection is available for all signals. In addition to have a good return path for all signals this large ground pad can be used for cooling.



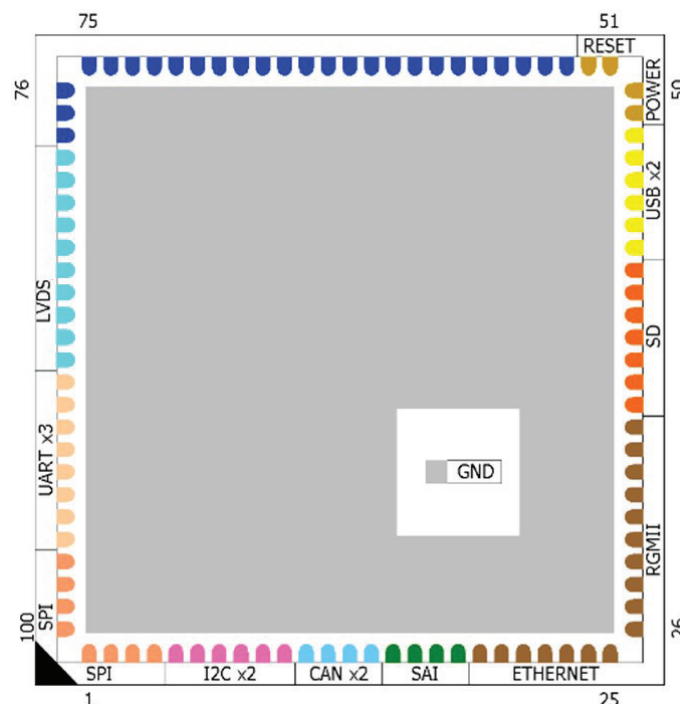
Easy Wiring - Even 2-layer printed circuit boards can be used.

With a solid ground plane on the bottom layer, high speed signals can be routed on the top layer at a defined impedance. However, this is only possible if a peripheral or plug can be connected directly without crossing other routes.

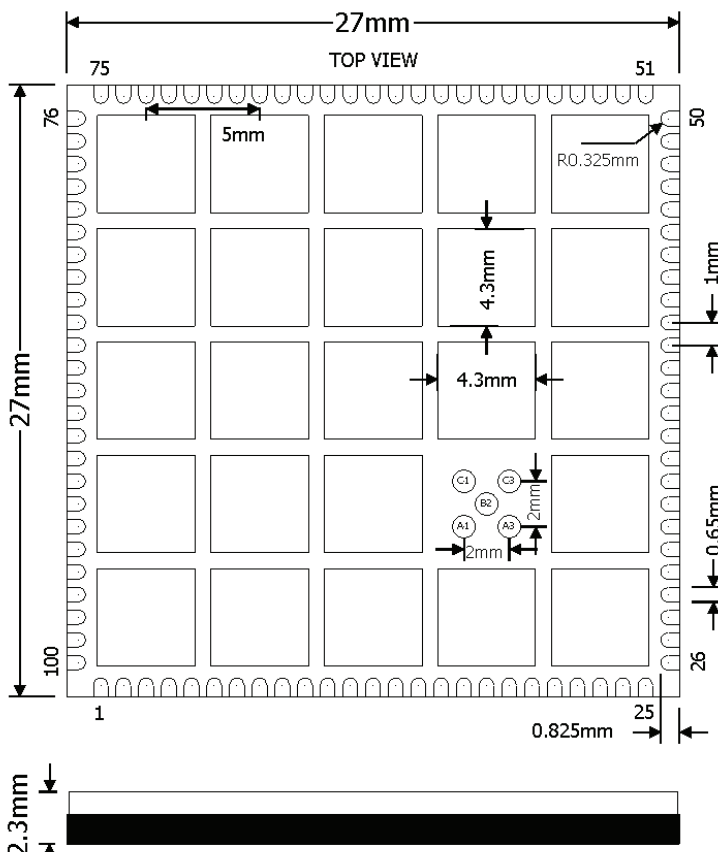
Advanced Soldering

Using a large solder pad underneath the component has not only electrical and thermal advantages. It is also used to hold the component at a defined height during soldering, without the solder being compressed by the weight of the components, which could result in short circuits.

Standard Contact Assignments

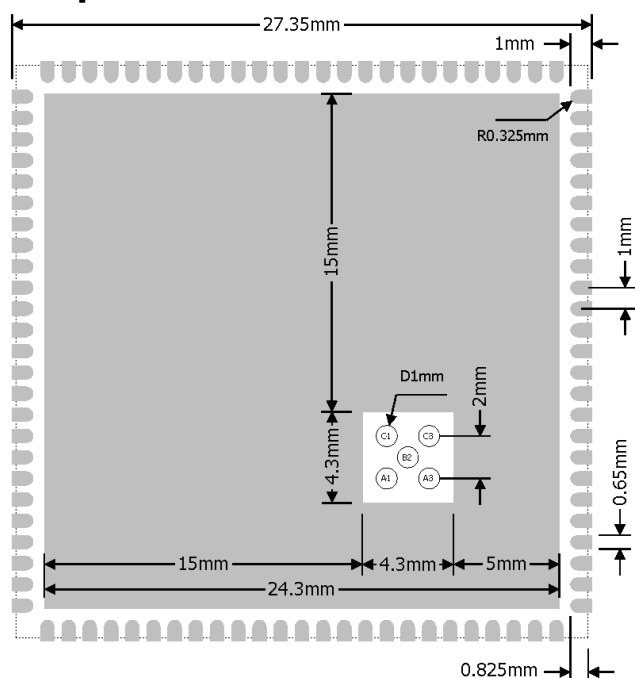


Package Information

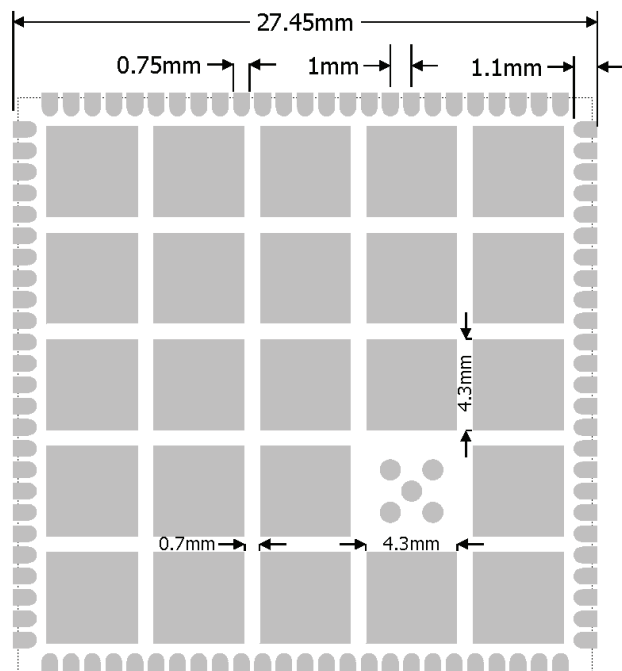


Layout Guidelines

Land pattern

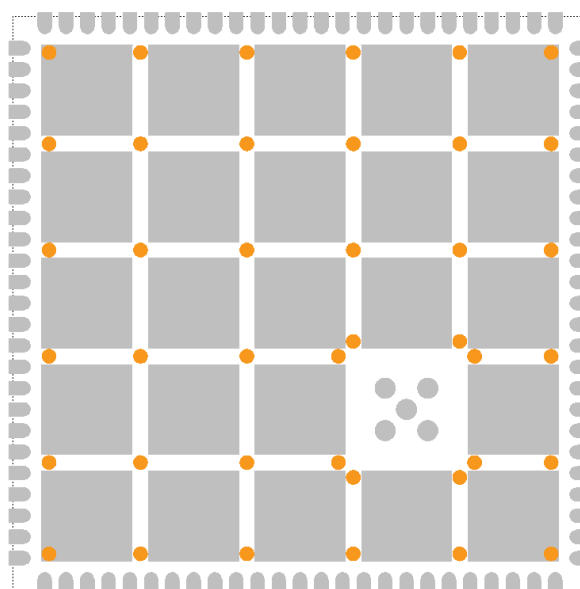


See figure above for the suggested module layout. The five 1mm pads in the square GND pad cutout can be omitted if no JTAG Boundary Scan test is used. The solder mask openings are shown below.



The ground pad solder mask on the bottom side of the QSCOM module is divided into sections for a better reliability of the solder joint and self-alignment of the component.

If the via holes used on the application board have a diameter larger than 0.3 mm, it is recommended to mask the via holes to prevent solder wicking through the via holes. Solders have a habit of filling holes and leaving voids in the thermal pad solder junction, as well as forming solder balls on the other side of the application board which can in some cases be problematic. The 0.7mm wide solder mask stripes can be used to arrange the vias as shown here:

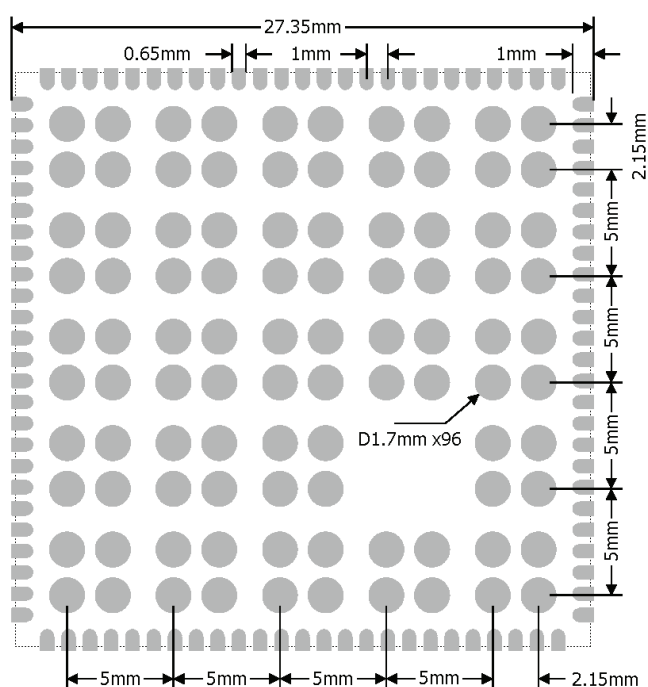


Soldering Recommendations

Ka-Ro QSCOM modules are compatible with industrial standard reflow profile for Pb-free solders. Ka-Ro will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendations should be taken as a starting point guide.

- Refer to technical documentations of particular solder paste for reflow profile configurations
- Avoid using more than one flow.
- A 150µm stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.
- A low residue, "no clean" solder paste should be used due to low mounted height of the component.

Recommended stencil design

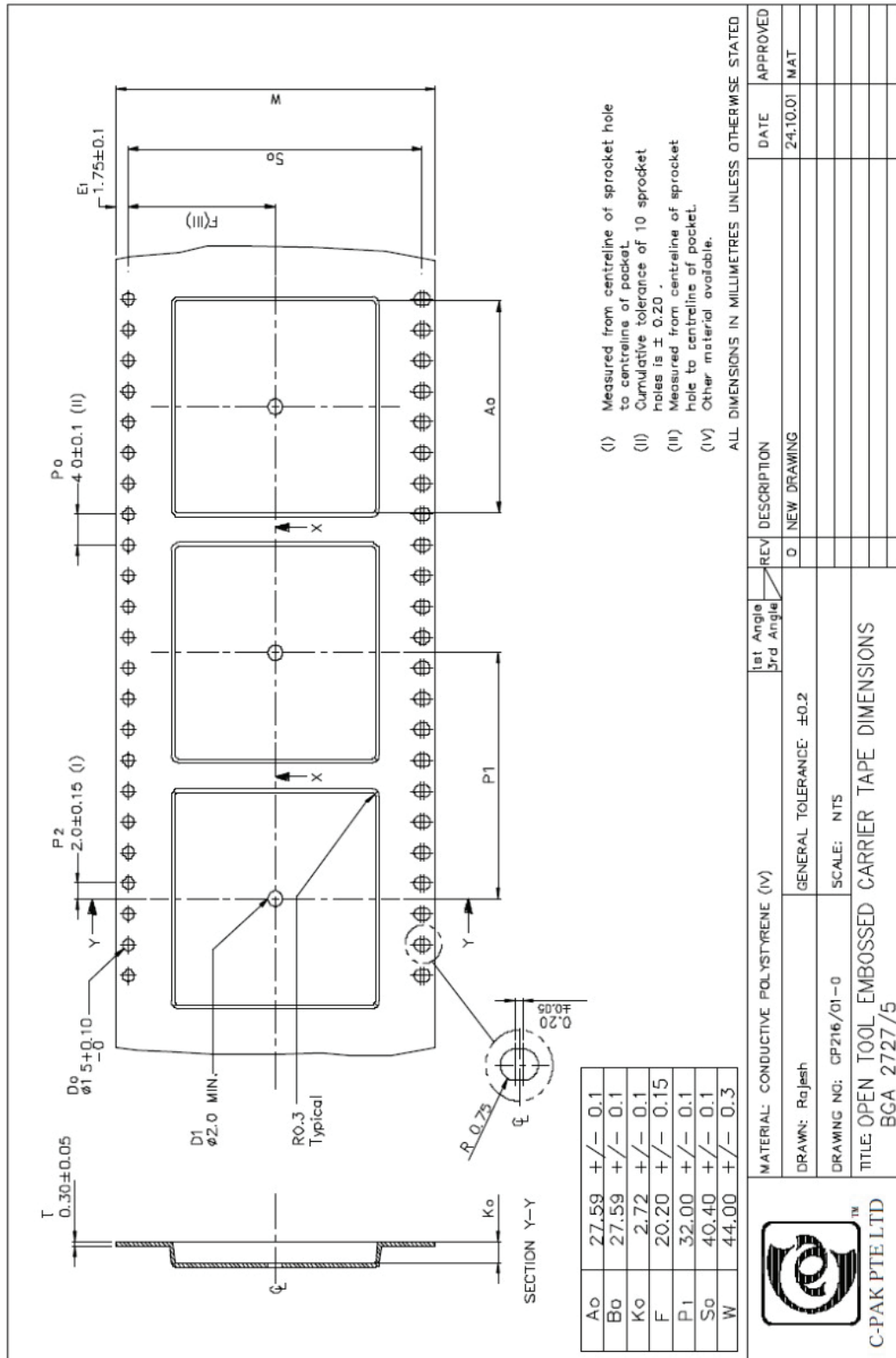


Aperture size of the stencil is 1:1 with the pad size. Four 1.7mm diameter bumps are used for each of the 4.3mm square GND pads sections giving a 50% solder paste padding. The lower component settling with this ensures that the pads at the edge are always soldered even at vertical misalignment by distortion or warping.

Thermal Considerations

A low residue, "no clean" solder paste should be used due to low mounted height of the component. The QSCOM module consume more than 1 W of DC power. In any application where high ambient temperatures for more than a few seconds can occur, it is important that a sufficient cooling surface is provided to dissipate the heat. The thermal pad at the bottom of the module must be connected to the application board ground planes by soldering. The application board should provide a number of vias under and around the pad to conduct the produced heat to the board ground planes, and preferably to a copper surface on the other side of the board in order to conduct and spread the heat. The module internal thermal resistance should in most cases be negligible compared to the thermal resistance from the module into air, and common equations for surface area required for cooling can be used to estimate the temperature rise of the module. Only copper planes on the circuit board surfaces with a solid thermal connection to the module ground pad will dissipate heat. For an application with high load the maximum allowed ambient temperature should be reduced due to inherent heating of the module, especially with small fully plastic enclosed applications where heat transfer to ambient air is low due to low thermal conductivity of plastic. The module measured on the evaluation board exhibits a temperature rise of about 20°C above ambient temperature. An insufficiently cooled module will rapidly heat beyond operating range in ambient room temperature.

Packaging



PINOUT (STM32MP2 pads named PA, PB, etc. can be used as GPIO ports)

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
1st SPI							
1	SPIA_NSS	PD5	TRACED1 SPI4_NSS HDP_HDP4 SAI1_D4	SAI1_FS_B - - -	TIM1_CH3N TIM4_CH2 OCTOSPIM_P1_IO1 -	- DCMIPP_D13 - -	
2	SPIA_MISO	PD4	TRACED0 SPI4_MISO HDP_HDP3 SAI1_D3	SAI1_SD_B - - -	TIM1_CH4N TIM4_CH1 OCTOSPIM_P1_IO0 -	- DCMIPP_D14 - -	
3	SPIA_MOSI	PD6	TRACED2 SPI4_MOSI HDP_HDP5 -	SAI1_SCK_B MDF1_SDI2 - -	TIM1_CH2N TIM4_CH3 OCTOSPIM_P1_IO2 -	- DCMIPP_D12 - -	
4	SPIA_SCK	PD7	DEBUG_TRACED3 SPI4_SCK SPI1_RDY -	SAI1_MCLK_B MDF1_CK12 - -	TIM1_CH1N TIM4_CH4 OCTOSPIM_P1_IO3 -	- DCMIPP_D11 - -	
I2C							
5	I2CA_SCL	PB5	- I2S2_MCK UART4_DE/UART4_RTS	SAI4_SD_B - - -	- I2C2_SCL OCTOSPIM_P2_IO5 -	FMC_D8/FMC_DA8 I3C2_SCL SDMMC3_D123DIR -	
6	I2CA_SDA	PB4	- SPI2_RDY UART4_CTS	SAI4_FS_B TIM14_CH1 - -	- I2C2_SDA OCTOSPIM_P2_IO4 -	I3C2_SDA - -	
7	INTA	PD15	SPI1_RDY - -	DSIHOST_TE FDCAN1_TX -	TIM1_BKIN2 TIM5_ETR I2C7_SCL FMC_D3/FMC_DA3	SDMMC3_CKIN DCMIPP_D0 -	
8	I2CB_SCL	PG6	DEBUG_TRACED4 HDP_HDP4 SPI5_SCK I2S1_CK/SPI1_SCK	- - - TIM2_CH4	- - - -	- LTDC_R6 DCMIPP_HSYNC -	GPIO I2C bit-banging
9	I2CB_SDA	PG5	DEBUG_TRACED3 HDP_HDP3 - USART6_DE/USART6_RTS	- - - TIM2_CH3	- - - -	- LTDC_R5 DCMIPP_PIXCLK -	GPIO I2C bit-banging
10	INTB	PD14	- I2S1_MCK -	- - FDCAN1_RX	TIM11_CH1 - I2C7_SDA FMC_D4/FMC_DA4	SDMMC3_D3 DCMIPP_D1 -	
CAN							
11	CANA_RX	PB11	- I2S3_MCK -	- USART1_CTS/USART1_NSS FDCAN1_RX	- TIM12_CH2 OCTOSPIM_P2_NCLK OCTOSPIM_P2_NCS2	FMC_D14/FMC_DA14 OCTOSPIM_P1_NCS2 -	
12	CANA_TX	PB9	SPI3_RDY - -	- USART1_DE/USART1_RTS FDCAN1_TX	- TIM10_CH1 OCTOSPIM_P2_DQS OCTOSPIM_P2_NCS2	FMC_D13/FMC_DA13 - -	
13	CANB_RX	PI10	SAI1_SCK_A I2S1_CK/SPI1_SCK SPDIFRX_IN0	FDCAN2_RX MDF1_CCK0 -	TIM4_CH1 - -	FMC_D12/FMC_DA12 DSIHOST_TE -	
14	CANB_TX	PI9	- I2S2_SDO/SPI2_MOSI -	FDCAN2_TX - -	TIM16_BKIN - FMC_NWAIT	DSIHOST_TE LTDC_B0 -	
SAI							
15	SAI_TX	PD1	- HDP_HDP1 I2S1_SDI/SPI1_MISO SAI1_CK2	- SAI4_SD_A UART7_DE/UART7_RTS TIM15_CH1	TIM1_BKIN - OCTOSPIM_P1_NCLK OCTOSPIM_P1_NCS2	OCTOSPIM_P2_NCS2 DCMIPP_HSYNC -	
16	SAI_RX	PI3	- - LPTIM1_IN2	SAI4_SD_B - USART1_CTS/USART1_NSS	TIM8_CH2 - -	- LTDC_B6 DCMIPP_D14 -	
17	SAI_SCK	PD2	HDP_HDP2 I2S1_WS/SPI1_NSS SAI1_CK1	SAI4_SCK_A UART7_CTS TIM15_BKIN	TIM1_ETR - OCTOSPIM_P1_DQS OCTOSPIM_P1_NCS2	- DCMIPP_VSYNC -	

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
18	SAI_FS	PD0	DEBUG_TRACECLK HDP_HDP0 - SAI1_D2	- SAI4_FS_A UART7_RX TIM15_CH2	- - OCTOSPIM_P1_CLK -	DCMIPP_PIXCLK - -	
ETHERNET 1							
19	ENET_RST	PB2	- I2S2_SDO/SPI2_MOSI -	- MDF1_CK13 TIM17_BKIN TIM16_BKIN SAI3_MCLK_A -	- - OCTOSPIM_P2_IO2 -	- - -	
20	ENET_CK125	PH9	- -	- USART6_RX TIM15_CH1N -	ETH1_RGMII_CLK125 ETH1_MII_RX_ER -	- -	
21	ENET_INT	PF5	- -	SAI3_MCLK_A USART6_TX TIM4_CH3 -	ETH1_MDIO ETH1_CLK ETH2_PHY_INTN ETH1_PHY_INTN -	LTDC_B6 -	
22	ENET_MDIO	PA10	- SPI4_MISO -	SAI2_SD_B USART2_RX LPTIM5_IN1 SAI3_SCK_A -	TIM2_CH2 - ETH1_MDIO -	LTDC_R6 DCMIPP_D15/PSSI_D15 -	
23	ENET_MDC	PF4	- RTC_OUT2 -	USART6_RX TIM4_CH4 -	ETH1_MDC ETH2_CLK ETH2_PPS_OUT ETH1_PPS_OUT -	LTDC_B7 -	
24	ENET_RXC	PA14	- SPI8_NSS LPTIM2_CH2 -	SAI4_FS_B MDF1_CCK1 -	- ETH1_RXC/REF_CLK -	- -	
25	ENET_RX_CTL	PA11	- SPI8_SCK LPTIM2_CH1 -	SAI4_SD_B -	- ETH1_RX_CTL/CRS_DV -	- -	
26	ENET_RXD0	PF1	- SPI8_MISO LPTIM2_IN2 -	SAI4_SCK_B USART2_CK -	- ETH1_RXD0 -	- -	
27	ENET_RXD1	PC2	- SPI8_MOSI LPTIM2_IN1 -	SAI4_MCLK_B MDF1_SDI3 USART2_DE/USART2_RTS -	- ETH1_RXD1 -	- -	
28	ENET_RXD2	PH12	- I2S3_WS/SPI3_NSS -	- -	TIM10_CH1 - ETH1_RXD2 -	- -	
29	ENET_RXD3	PH13	- I2S3_CK/SPI3_SCK -	- TIM15_BKIN -	TIM11_CH1 - ETH1_RXD3 -	- -	
30	ENET_TX_CTL	PA13	- SPI8_RDY I2S3_MCK LPTIM2_ETR -	MDF1_CK13 USART2_CTS/USART2_NSS -	I2C7_SMBA ETH1_TX_CTL/TX_EN -	- -	
31	ENET_TXC	PC0	- LPTIM1_CH1 -	SAI3_MCLK_B USART6_TX -	DCMIPP_D0 ETH2_RMII_REF_CLK ETH1_MII_TX_CLK -	ETH1_RGMII_GTX_CLK LTDC_G7 -	
32	ENET_TXD3	PH11	- -	SAI3_FS_A -	ETH2_MDIO ETH1_TXD3 -	- -	
33	ENET_TXD2	PH10	- I2S1_CK/SPI1_SCK -	TIM15_CH2 SAI3_SCK_A - TIM15_CH1 -	ETH2_MDC ETH1_TXD2 -	- -	
34	ENET_TXD1	PC1	- I2S3_SDO/SPI3_MOSI -	- USART2_TX -	I2C7_SCL ETH1_TXD1 -	- -	
35	ENET_TXD0	PA15	- I2S3_SDI/SPI3_MISO -	USART2_RX -	I2C7_SDA ETH1_TXD0 -	- -	
SD							
36	SD_CD	PA4	- -	- USART2_TX FDCAN2_TX -	TIM2_CH1 LTDC_R1	ETH1_PTP_AUX_TS	

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
37	SD_D1	PE5	DEBUG_TRACED1 LPTIM2_IN2 I2S1_WS/SPI1_NSS I2S3_WS/SPI3_NSS	SAI1_FS_B - USART3_DE/USART3_RTS FDCAN1_RX	- - SDMMC1_D1 -	- - - -	
38	SD_D0	PE4	DEBUG_TRACED0 LPTIM2_IN1 I2S1_SDO/SPI1_MOSI I2S3_SDI/SPI3_MISO	SAI1_SD_B - USART3_CTS/USART3_NSS FDCAN1_TX	- - SDMMC1_D0 -	- - - -	
39	SD_CLK	PE3	DEBUG_TRACECLK - SPI1_RDY I2S3_CK/SPI3_SCK	SAI1_MCLK_B - USART3_TX -	TIM11_CH1 - SDMMC1_CK -	- - - -	
40	SD_CMD	PE2	LPTIM2_ETR I2S1_SDI/SPI1_MISO I2S3_SDO/SPI3_MOSI	SAI1_SCK_B - - -	TIM10_CH1 - SDMMC1_CMD -	- - - -	
41	SD_D3	PE1	DEBUG_TRACED3 LPTIM2_CH2 I2S1_MCK I2S3_MCK	- - USART3_RX -	- - SDMMC1_D3 -	- - - -	
42	SD_D2	PE0	DEBUG_TRACED2 LPTIM2_CH1 I2S1_CK/SPI1_SCK SPI3_RDY	- - USART3_CK -	- - SDMMC1_D2 -	- - - -	

USB

43	USBA_VBUS	UCPD1_CC2					
44	USBA_DN	USBH_HS_DM					
45	USBA_DP	USBH_HS_DP					
46	USBB_VBUS	UCPD1_CC1					
47	USBB_DN	USB3DR_DM					
48	USBB_DP	USB3DR_DP					

POWER SUPPLY & RESET

49	VIN	3.3V power supply input					
50							
51	NRST	Open drain reset to reset of external devices, or to reset the device. Connected to STM32MP2 NRST and PCA9450 POR_B, 10K-PU					
52	BOOT_MODE	Connected to STM32MP2 BOOT1, 10K-PU. BOOT[0,2,3]=L					H: Boot from eMMC L: Boot from USB

MISC

53		PB15	- LPTIM1_IN2 SPI5_SCK -	SAI2_SD_B UART5_RX - TIM3_CH2	TIM5_CH1 - ETH1_PPS_OUT -	FMC_A18 LTDC_R4 DCMIPP_D8 -	
54		PF3	- - - -	SAI2_SCK_B MDF1_CCK0 - TIM3_CH4	TIM8_BKIN2 ETH1_CLK ETH2_PPS_OUT -	FMC_A20 LTDC_R6 DCMIPP_HSYNCR -	
55		PG3	- LPTIM1_ETR SPI5_MOSI -	SAI2_FS_B - - TIM3_CH3	TIM8_ETR ETH2_CLK ETH2_PHY_INTN -	FMC_A19 LTDC_R5 DCMIPP_PIXCLK -	
56		PG2	- RTC_REFIN I2S3_MCK -	SAI2_FS_A - USART3_CK -	TIM5_CH3 - ETH2_MII_TX_CLK ETH2_RGMII_CLK125	FMC_CLK LTDC_HSYNCR - -	

MIPI-CSI

57	CSI1_D1_P	CSI_D1P					
58	CSI1_D1_N	CSI_D1N					
59	CSI1_D0_P	CSI_D0P					
60	CSI1_D0_N	CSI_D0N					
61	CSI1_CLK_P	CSI_CKP					
62	CSI1_CLK_N	CSI_CKN					

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
ETHERNET 2							
63	ENET2_TXC	PF7	- SPDIFRX_IN1 -	SAI3_SD_A - TIM2_ETR	- ETH2_GTX_CLK ETH2_MII_TX_CLK	- LTDC_R1 -	
64	ENET2_TD3	PC10	- I2S3_SDO/SPI3_MOSI -	- LPTIM4_ETR SAI2_SCK_A	TIM8_CH4 USBH_HS_VBUSEN ETH2_TXD3 USB3DR_VBUSEN	FMC_A23 LTDC_G3 DCMIPP_D6	
65	ENET2_TD2	PC9	- RCC_MCO_1 I2S3_SDI/SPI3_MISO -	- SAI2_SCK_A TIM13_CH1	TIM8_CH4N USBH_HS_OVRCUR ETH2_TXD2 USB3DR_OVRCUR	FMC_A22 LTDC_G2 DCMIPP_D7	
66	ENET2_TD1	PC8	- LPTIM1_ETR -	SAI3_SCK_B USART6_CTS/USART6_NSS	TIM8_CH2 -	LTDC_B3 DCMIPP_D2	
67	ENET2_TD0	PC7	- -	SAI3_SD_B -	TIM8_CH2N -	LTDC_B4 DCMIPP_D1	
68	ENET2_TX_CTL	PC4	- -	SAI3_FS_B -	- ETH2_TX_CTL/TX_EN	ETH1_RGMII_CLK125 LTDC_R0	
69	ENET2_RX_CTL	PC3	- LPTIM1_IN2 I2S3_WS/SPI3_NSS -	-- USART6_DE/USART6_RTS FDCAN2_TX	- ETH2_RX_CTL/CRS_DV ETH1_MII_RX_ER	LTDC_G6 DCMIPP_D3	
70	ENET2_RXC	PF6	- RTC_OUT2 SAI3_MCLK_B	- USART6_CK TIM12_CH1	- ETH2_RX_CLK/REF_CLK	LTDC_B0	
71	ENET2_RD3	PC11	- LPTIM1_CH1 SPI5_NSS	SAI2_MCLK_A UART5_DE/UART5_RTS USART3_DE/USART3_RTS	TIM5_ETR -	FMC_NBL1 LTDC_R2 DCMIPP_D10	
72	ENET2_RD2	PF9	- -	SAI2_SD_A -	- ETH2_RXD2 ETH2_MDIO		
73	ENET2_RD1	PC12	- LPTIM1_CH2 -	MDF1_CK12 -	TIM8_CH3 -	LTDC_G1 DCMIPP_D5/DCMI_D5/PSS I_D5	
74	ENET2_RD0	PG0	- LPTIM1_IN1 -	MDF1_SDI2 -	TIM8_CH3N -	LTDC_G5 DCMIPP_D4/DCMI_D4/PSS I_D4	
75	ENET2_MDIO	PC5	- SPDIFRX_IN1 -	MDF1_SDI1 -	TIM8_CH1N -	FMC_A25 ETH1_PPS_OUT LTDC_DE	
76	ENET2_MDC	PG4	- SPI5_MISO SAI3_FS_B	- LPTIM4_IN1	TIM8_BKIN ETH2_PPS_OUT ETH2_MDC	FMC_A21 LTDC_R7 DCMIPP_VSYNC/DCMI_VSY NC/PSSI_RDY	
Display Control							
77	LCD_EN	PH5	- -	SAI2_FS_A -	UART7_RX -	USBH_HS_VBUSEN ETH2_PTP_AUX_TS	
78	LCD_BL	PF13	- DEBUG_TRACED0 HDP_HDP0 AUDIOCLK USART6_TX	TIM2_CH1 I2S2_WS/SPI2_NSS USART3_CTS/USART3_NSS	LTDC_G1 USB3DR_VBUSEN TIM3_CH3	LTDC_R2	
LVDS DISPLAY							
79	CSI_CKP LVDS_TX3P	LVDS_D3P					
80	DSI_DP3 LVDS_TX3N	LVDS_D3N					
81	DSI_DN3 LVDS_TX2P	LVDS_D2P					
82	DSI_DN3 LVDS_TX2N	LVDS_D2N					

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
83	DSI_DP1 LVDS_TX1P		LVDS_D1P				
84	DSI_DN1 LVDS_TX1N		LVDS_D1N				
85	DSI_DP0 LVDS_TX0P		LVDS_D0P				
86	DSI_DN0 LVDS_TX0N		LVDS_D0N				
87	DSI_CKP LVDS_CLKP		LVDS_D4P				
88	DSI_CKN LVDS_CLKN		LVDS_D4N				

UART

89	UARTA_RXD	PB6	- I2S2_SDI/SPI2_MISO UART4_RX	SAI4_SCK_B - -	- OCTOSPIM_P2_IO6 -	FMC_D9/FMC_DA9 SDMMC3_D0DIR -	
90	UARTA_TXD	PB7	- I2S3_CK/SPI3_SCK UART4_TX	SAI4_MCLK_B - -	- TIM12_CH1 OCTOSPIM_P2_IO7 -	FMC_D10/FMC_DA10 SDMMC3_CDIRE -	
91	UARTB_RXD	PI7	- -	- USART3_RX TIM2_CH1	- TIM3_CH2 -	- LTDC_HSYNC	
92	UARTB_TXD	PI6	- RCC_MCO_1 -	- USART3_TX TIM2_ETR	- TIM3_CH1 -	- LTDC_VSYNC -	
93	UARTC_RXD	PG10	- DEBUG_TRACED8 HDP_HDP0 -	- UART5_RX -	- TIM8_CH4N -	- LTDC_G4 DCMIPP_D4/DCMI_D4/PSS I_D4 -	
94	UARTC_TXD	PG9	- DEBUG_TRACED7 -	- UART5_TX -	- TIM5_CH4 -	- LTDC_G3 DCMIPP_D3/DCMI_D3/PSS I_D3 -	
95	UARTC_CTS	PG1	- LPTIM1_IN1 I2S3_MCK -	SAI2_SD_A UART5_CTS USART3_CTS/USART3_NSS -	TIM5_CH4 ETH2_MII_RX_ER ETH2_MII_RXD3	FMC_NBL0 LTDC_VSYNC DCMIPP_D11/DCMI_D11/P SSI_D11 -	CTS/RTS input signal
96	UARTC_RTS	PG8	- DEBUG_TRACED6 HDP_HDP6 SPI5_RDY SPI1_RDY	USART6_CK UART5_DE/UART5_RTS -	TIM5_CH3 -	- LTDC_G2 DCMIPP_D2/DCMI_D2/PSS I_D2 -	RTS/CTS output signal

2nd SPI

97	SPIB_NSS	PA8	- LPTIM2_CH2 -	SAI1_FS_B - USART1_CK -	USART2_RX -	LTDC_B2 DCMIPP_D4 -	GPIO SPI bit-banging
98	SPIB_MISO	PD12	- I2S2_SDI/SPI2_MISO SPDIFRX_IN2 -	- -	- TIM4_ETR SDMMC3_CMD FMC_D6/FMC_DA6 -	FMC_D1/FMC_DA1 -	GPIO SPI bit-banging
99	SPIB_MOSI	PG11	- DEBUG_TRACED9 HDP_HDP1 -	- -	- TIM8_CH4 -	- LTDC_G5 DCMIPP_D5 -	GPIO SPI bit-banging
100	SPIB_SCK	PB13	- -	FDCAN1_TX SAI1_SD_B -	- -	FMC_D0/FMC_DA0 -	GPIO SPI bit-banging

Pins used for manufacturing and debugging – leave unconnected

PIN	(SPM32MP2 PAD NAME)	PIN	(SPM32MP2 PAD NAME)	PIN	(SPM32MP2 PAD NAME)
C1	JTAG_TDI (JTDI)			C3	JTAG_TCK (JTCK_SWCLK)
		B2	JTAG_TDO (JTDO_TRACESWO)		
A1	JTAG_TRST_B (NJTRST)			A3	JTAG_TMS (JTMS_SWDIO)

Onboard peripherals wiring

USED FOR		MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-14	Remarks
eMMC	CMD	PE15	-	SAI1_SCK_A	TIM1_CH1N	SDMMC2_CMD	10K-PU
			-	-	-	-	
			-	TIM15_CH1N	FMC_NOE	-	
	CLK	PE14	-	SAI1_MCLK_A	TIM1_BKIN	SDMMC2_CK	10K-PU
			-	-	-	-	
			-	TIM15_BKIN	FMC_NWE	-	
	DAT0	PE13	-	SAI1_SD_A	TIM1_CH2N	SDMMC2_D0	10K-PU
			-	-	-	-	
			-	TIM15_CH1	FMC_RNB	-	
	DAT1	PE11	-	SAI1_FS_A	TIM1_CH3N	SDMMC2_D1	
eMMC			-	-	-	-	
			SAI4_D3	TIM15_CH2	FMC_A16/FMC_CLE	-	
	DAT2	PE8	SPI4_MOSI	SAI4_MCLK_A	TIM1_CH1	SDMMC2_D2	
			-	MDF1_CKIO	-	-	
			SAI4_CK1	-	FMC_A17/FMC_ALE	-	
	DAT3	PE12	SPI4_NSS	SAI4_SCK_A	TIM1_CH2	SDMMC2_D3	
			-	MDF1_SDI0	-	-	
			SAI4_CK2	USART1_RTS	FMC_NE2	-	
	DAT4	PE10	SPI4_SCK	SAI4_SD_A	TIM1_CH3	SDMMC2_D4	
			-	USART1_CTS	-	SDMMC2_CKIN	
eMMC			SAI4_D1	-	FMC_NE3	-	
	DAT5	PE9	SPI4_MISO	SAI4_FS_A	TIM1_CH4	SDMMC2_D5	
			-	USART1_CK	-	SDMMC2_CDIR	
			SAI4_D2	-	FMC_D0/FMC_DA0	-	
	DAT6	PE6	SPI4_RDY	SPDIFRX_IN2	TIM1_ETR	SDMMC2_D6	
			-	USART1_TX	-	SDMMC2_D0DIR	
			-	-	FMC_D1/FMC_DA1	-	
	DAT7	PE7	-	SPDIFRX_IN3	TIM1_CH4N	SDMMC2_D7	
			-	USART1_RX	-	SDMMC2_D123DIR	
			SAI4_D4	-	TIM14_CH1	-	
PMIC PCA9450A	SDA	PI1	DEBUG_TRACED15	-	TIM8_CH3N	-	1K-PU
			HDP_HDP7	-	I2C1_SDA	LTDC_B4	
			-	-	I3C1_SDA	DCMIPP_D8/PSSI_D8	
	SCL	PG13	DEBUG_TRACED11	-	TIM8_CH2N	-	10K-PU
			HDP_HDP3	MDF1_CKIO	I2C1_SCL	LTDC_G7	
			SPI7_SCK	-	I3C1_SCL	DCMIPP_D7/PSSI_D7	
	IRQ_B	PD11	DEBUG_TRACED7	UART4_TX	TIM1_CH1	SDMMC1_CKIN	10K-PU
PMIC PCA9450A			I2S1_CK/SPI1_SCK	MDF1_CKIO	-	DCMIPP_D7/DCMI_D7/PSSI_D7	
			SAI1_MCLK_A	-	OCTOSPIM_P1_IO7	-	
	POR_B	NRST			SDMMC1_D4		10K-PU
	PMIC_ON_REQ	PWR_ON					
	PMIC_STBY_REQ	PWR_LP					
	WDOG_B	PD8	DEBUG_TRACED4	UART4_CTS	TIM1_CH4	SDMMC1_D123DIR	10K-PU
			SPI4_RDY	MDF1_SDI1	TIM4_ETR	DCMIPP_D10/PSSI_D10	
PMIC PCA9450A			I2S1_MCK	-	OCTOSPIM_P1_IO4	-	
			SAI1_FS_A	-	SDMMC1_D7		