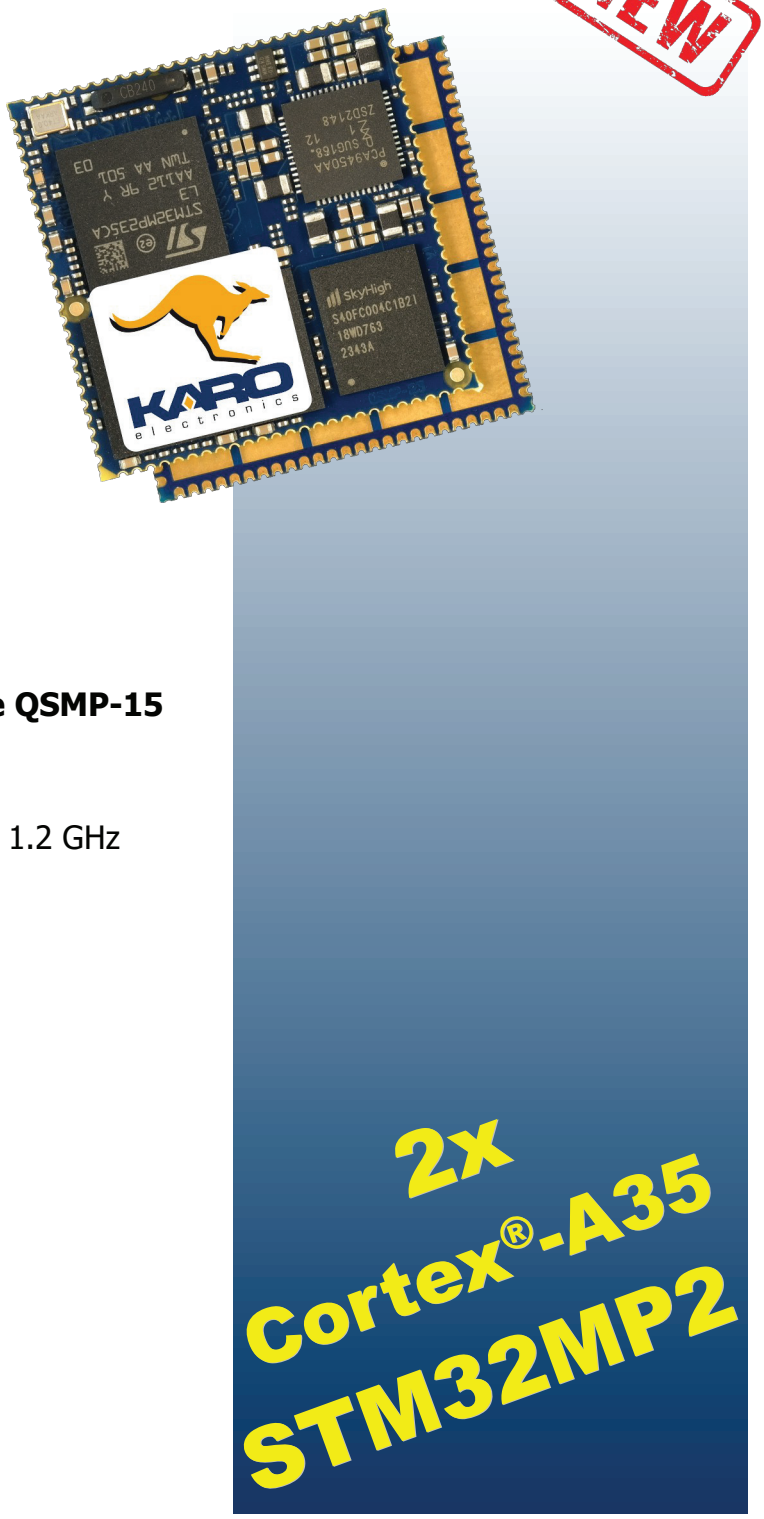
QSMP-20

QFN Style
Solder-Down
Computer On Module



- 27mm square
- 2.6mm total height
- QS family pin-compatible
- Solder-down version
- QFN type lead style
  - 1mm pitch
  - 100 pads
  - Thermal pad
- Visual solder joint inspection possible after soldering
- Single-sided assembly
- 3.3V power supply

Key Features

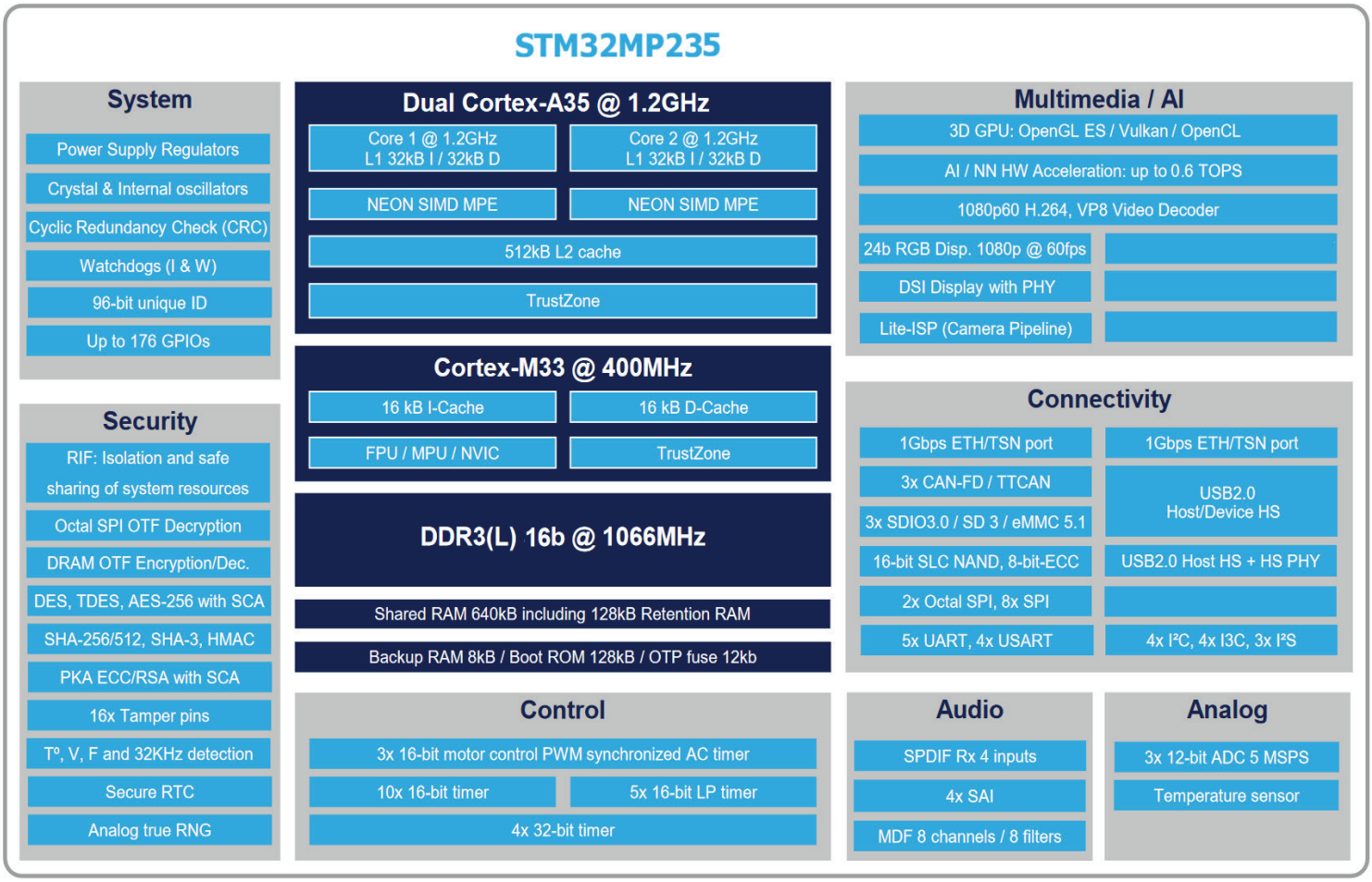
- **Drop-in, pin-compatible upgrade for the QSMP-15**
- Standard configuration with:
  - STM32MP235C Dual ARM® Cortex®-A35, 1.2 GHz
  - RAM 512 MB DDR3L
  - ROM 4 GB eMMC
  - Grade Industrial
  - Temperature -25°C to 85°C
- Connectivity
  - RGB Display Interface
  - MIPI DSI
  - 2x USB 2.0
  - 1x Gb Ethernet, RGMII
  - 1x eMMC/SD
  - 2x CAN-FD
  - 3x UART, 2x I²C, 2x SPI, PWM, SAI
  - Up to 82x 3.3V General Purpose I/O

OS Support

- Linux

Authorized Partner

Direct Insight Ltd
The Hayloft, Greatworth Hall, Greatworth, Banbury, Oxfordshire, OX17 2DH, UK
Phone: +44 1295 768800 | Fax: +44 1295 762499 | Web: www.directinsight.co.uk



QSMP-15 | QSMP-20 | QSMP-25 | Differentiating Features

	QSMP-15 STM32MP157	QSMP-20 STM32MP235	QSMP-25 STM32MP255
Primary Arm® Core	2x Cortex®-A7 650 MHz	2x Cortex®-A35 1.2 GHz	2x Cortex®-A35 1.5 GHz
Secondary Arm® Core	Cortex®-M4 250 MHz	Cortex®-M33 400 MHz	Cortex®-M33 400 MHz
RAM	512MB DDR3L	512MB DDR3L	1GB LPDDR4
ROM	4 GB eMMC	4 GB eMMC	4 GB eMMC
GPU	3D GPU	66 MTrg/s 400 MPix/s 12.8 GFlops	133 MTrg/s 800 MPix/s 25.6 GFlops
AI/ML/DSP	-	0.6 TOPS	1.2 TOPS
VPU	-	Decode	De-/Encode
Connectivity	USB 2.0	USB 2.0	USB 2.0, USB 3.0 or PCIe
Display Interface	RGB + MIPI-DSI	RGB + MIPI-DSI	LVDS
QS Size	100 pins 27mm square	100 pins 27mm square	108 pins 29mm square
Grade / Temperature	Industrial -25°C to 85°C	Industrial -25°C to 85°C	Industrial -40°C to 85°C

2026-05-04

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QSMP-20 Custom Options

	Standard	Options
RAM	512 MB DDR3L	256 MB / 1 GB
ROM	4 GB eMMC	8 GB
Temperature	-25°C to 85°C	-40°C to 85°C
MPU	MP235C	see below

MP2x1/x3/x5 Differentiating Features

	MP211 MP231 MP251	MP213 MP233 MP253	MP215 MP235 MP255
Cortex®-A35	1	1 2 2	1 2 2
GPU/NPU/VPU	-	- yes yes	- yes yes
Display Interface	- TTL TTL	- TTL TTL	TTL TTL/DSI TTL/DSI
FDCAN	-	2	2

MP21x/3x/5x Differentiating Features

	MP21x	MP23x	MP25x
Cortex®-A35	1.2/1.5 GHz	1.2/1.5 GHz	1.2/1.5 GHz
Cortex®-M33	300 MHz	400 MHz	400 MHz
Cortex®-M0+	-	-	200 MHz
L2 cache	128 kB	512 kB	512 kB
SRAM	64 kB	256 kB	256 kB
GPU/NPU	-	66 MTrg/s 400 MPix/s 12.8 GFlops	133 MTrg/s 800 MPix/s 25.6 GFlops
NPU	-	0.6 TOPS	1.2 TOPS
VPU	-	Decode	De-/Encode
Display Rotation	-	yes	yes
DDR3L Speed	800 MHz	933 MHz	933 MHz
SDRAM OTF en-/decryption	AES-256/192/128 SCA protection	AES-128	AES-128
SHA-512, SHA-3 HMAC (HASH1/2)	2	1	1
RNG (RNG1/2)	2	1	1
Tamper trigger via monitoring of voltages	yes	-	-
Secure isolation level	4	2	2
Encryption of the first stage boot loader	AES-256	AES-128	AES-128
Secure Boot Signature	ECDSA P-384 BrainpoolP384	P-256 P256	P-256 P256
Additional 384 authentication key	yes	-	-
Increased ROM code execution performance	yes	-	-

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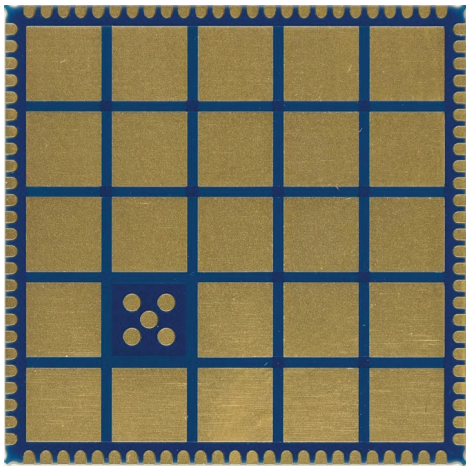
QFN Style Computer On Module Advantages

Defined Return Path

The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller formfactors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation may occur on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

When a module or component is used in a design, the supplier specifies the basis for such a layout. It's not only the pinout which should lead to an easy wiring without the need for crossings. He also has to provide a proper solution for the signal path back to the module. If this return path, mostly the ground plane, cannot be connected near the signal pin, the return current has to take another way and this may result in a loop area. The larger the area, the more radiation and EMI problems may occur.

Ka-Ro QSCOM modules uses a large ground pad on the bottom side. With this a defined ground plane connection is available for all signals. In addition to have a good return path for all signals this large ground pad can be used for cooling.



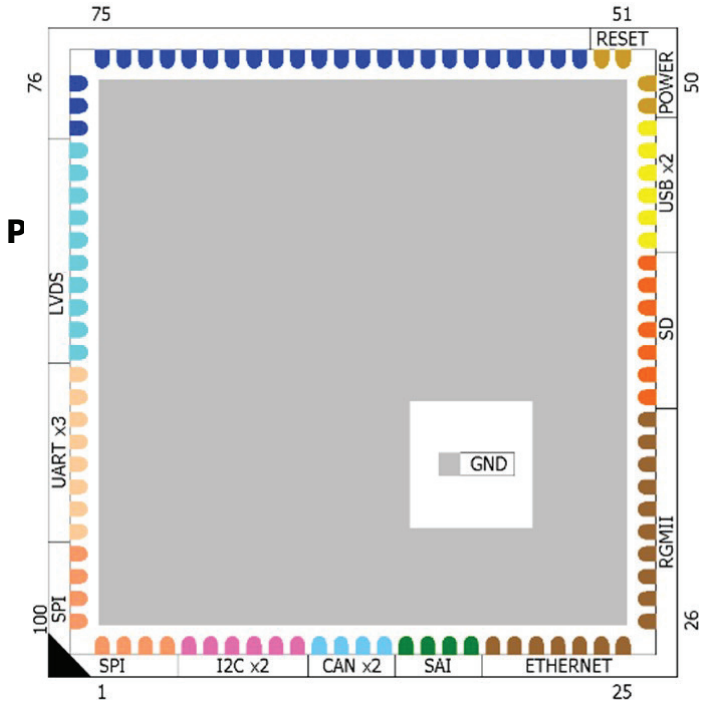
Easy Wiring - Even 2-layer printed circuit boards can be used.

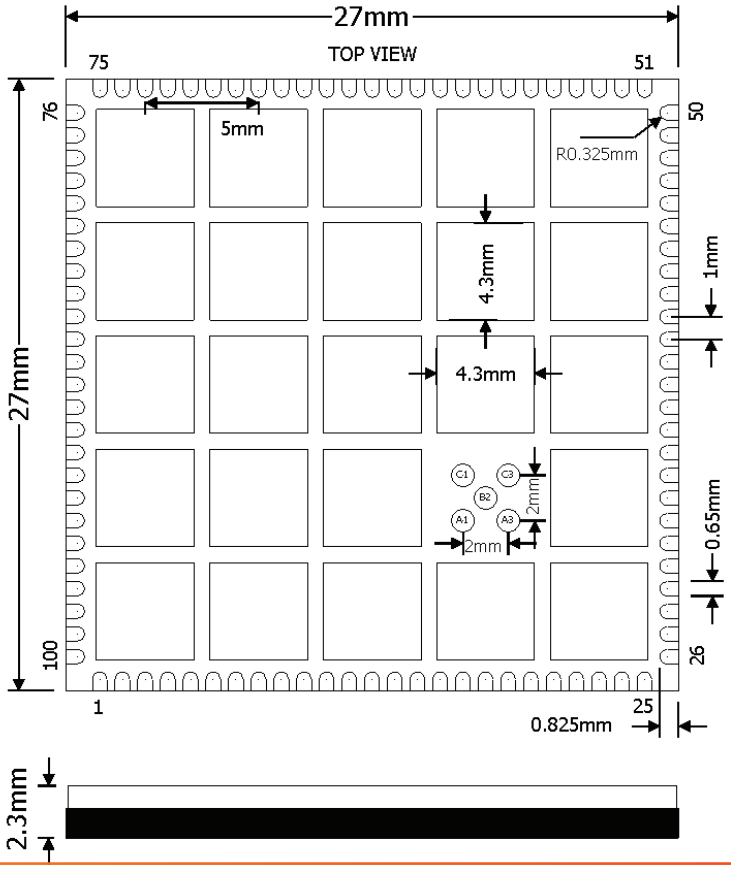
With a solid ground plane on the bottom layer, high speed signals can be routed on the top layer at a defined impedance. However, this is only possible if a peripheral or plug can be connected directly without crossing other routes.

Advanced Soldering

Using a large solder pad underneath the component has not only electrical and thermal advantages. It is also used to hold the component at a defined height during soldering, without the solder being compressed by the weight of the components, which could result in short circuits.

Standard Contact Assignments





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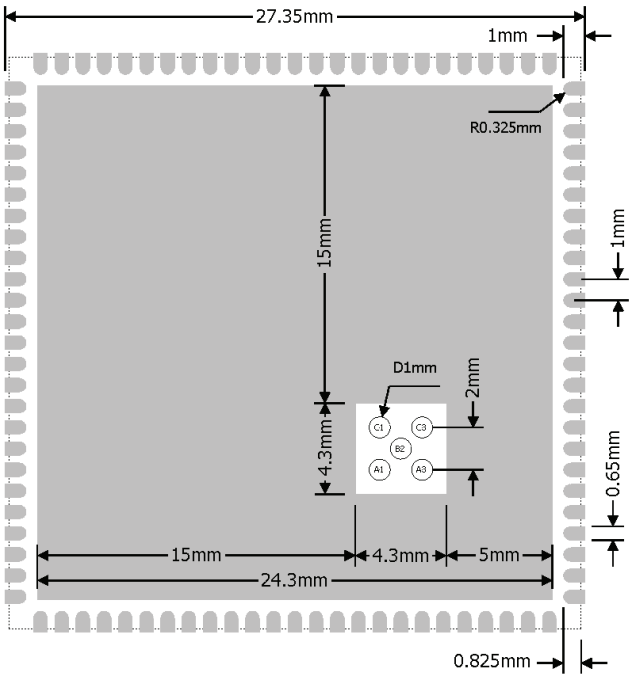
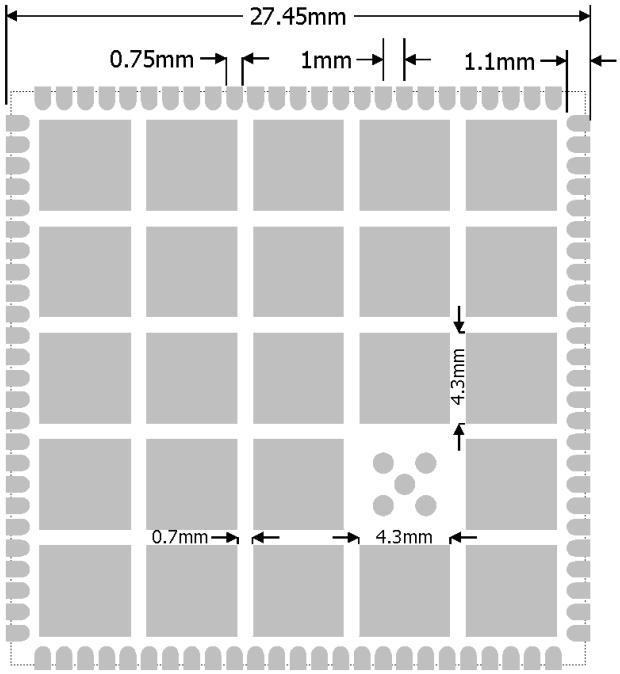
Layout Guidelines

Land pattern

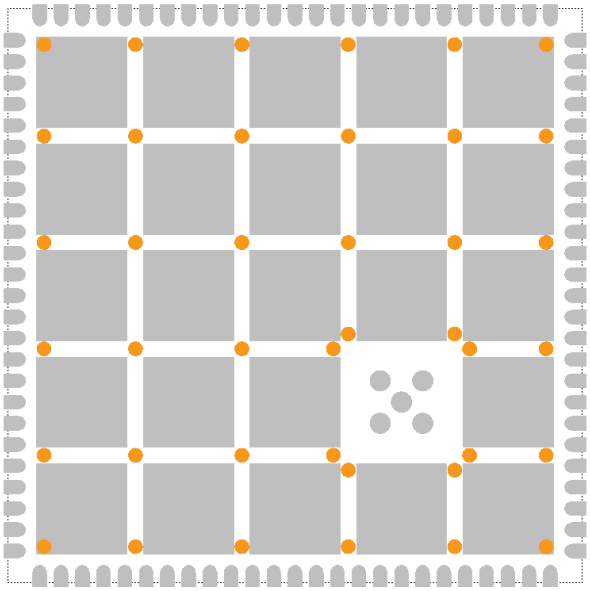


See figure above for the suggested module layout. The five 1mm pads in the square GND pad cutout can be omitted if no JTAG Boundary Scan test is used. The solder mask openings are shown below.



The ground pad solder mask on the bottom side of the QSCOM module is divided into sections for a better reliability of the solder joint and self-alignment of the component.

If the via holes used on the application board have a diameter larger than 0.3 mm, it is recommended to mask the via holes to prevent solder wicking through the via holes. Solders have a habit of filling holes and leaving voids in the thermal pad solder junction, as well as forming solder balls on the other side of the application board which can in some cases be problematic. The 0.7mm wide solder mask stripes can be used to arrange the vias as shown here:

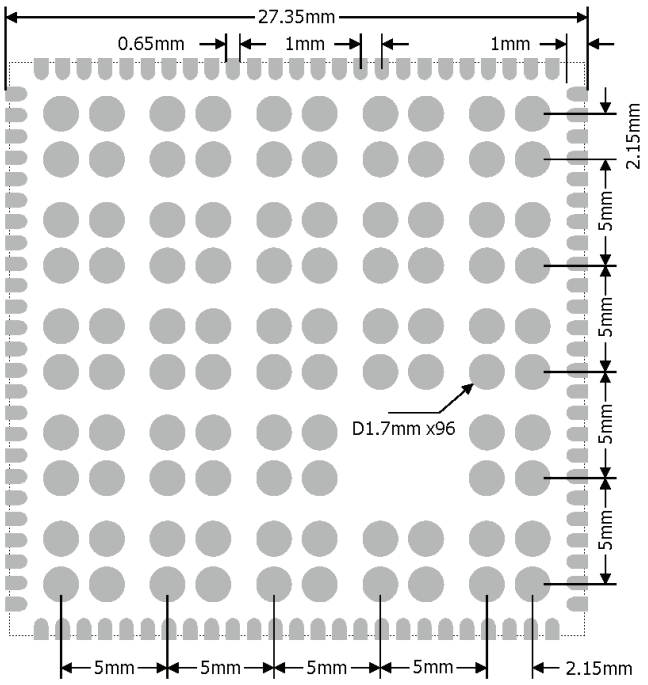


Soldering Recommendations

Ka-Ro QSCOM modules are compatible with industrial standard reflow profile for Pb-free solders. Ka-Ro will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendations should be taken as a starting point guide.

- Refer to technical documentations of particular solder paste for reflow profile configurations
- Avoid using more than one flow.
- A 150µm stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.
- A low residue, "no clean" solder paste should be used due to low mounted height of the component.

Recommended stencil design

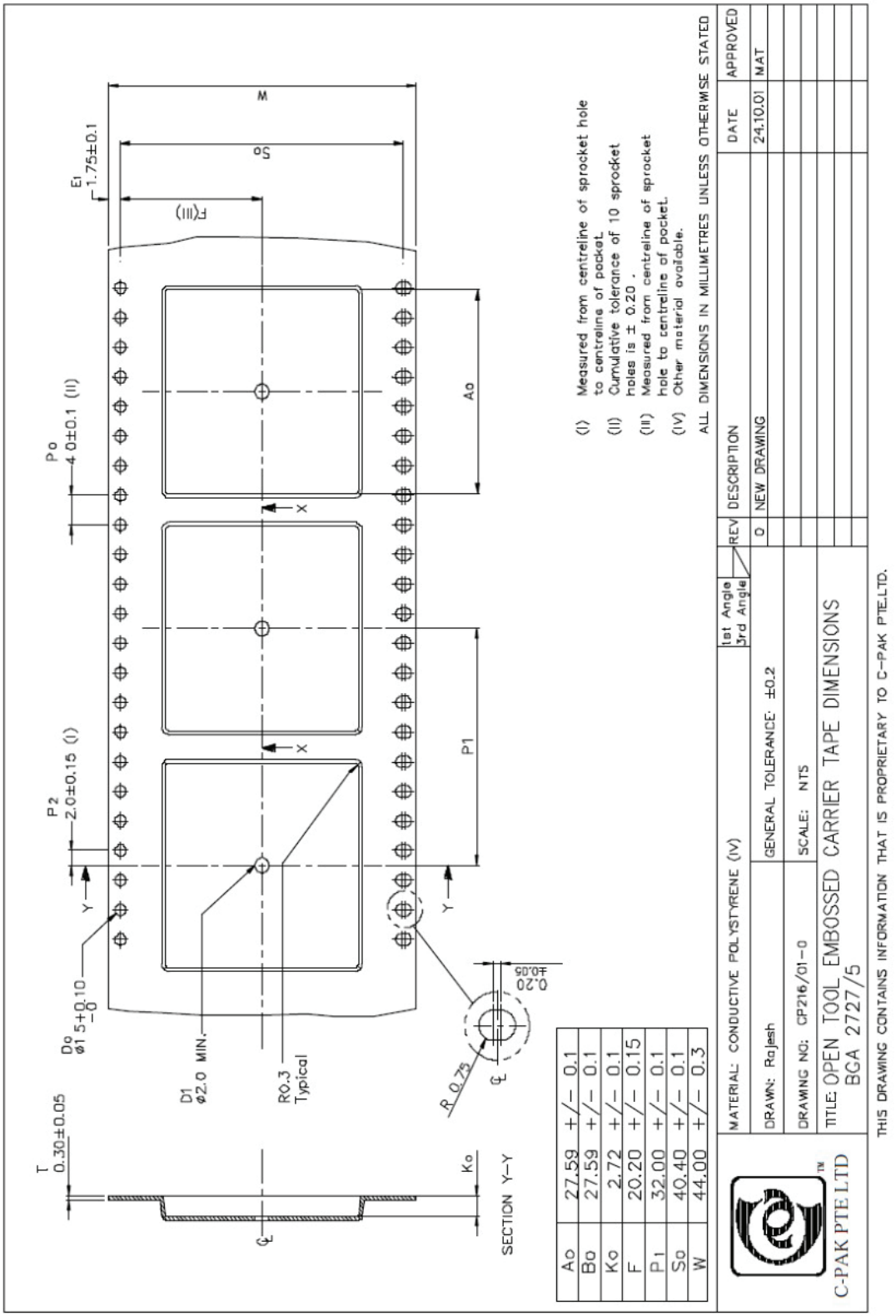


Aperture size of the stencil is 1:1 with the pad size. Four 1.7mm diameter bumps are used for each of the 4.3mm square GND pads sections giving a 50% solder paste padding. The lower component settling with this ensures that the pads at the edge are always soldered even at vertical misalignment by distortion or warping.

Thermal Considerations

A low residue, "no clean" solder paste should be used due to low mounted height of the component.The QSCOM module consume more than 1 W of DC power. In any application where high ambient temperatures for more than a few seconds can occur, it is important that a sufficient cooling surface is provided to dissipate the heat. The thermal pad at the bottom of the module must be connected to the application board ground planes by soldering. The application board should provide a number of vias under and around the pad to conduct the produced heat to the board ground planes, and preferably to a copper surface on the other side of the board in order to conduct and spread the heat. The module internal thermal resistance should in most cases be negligible compared to the thermal resistance from the module into air, and common equations for surface area required for cooling can be used to estimate the temperature rise of the module. Only copper planes on the circuit board surfaces with a solid thermal connection to the module ground pad will dissipate heat. For an application with high load the maximum allowed ambient temperature should be reduced due to inherent heating of the module, especially with small fully plastic enclosed applications where heat transfer to ambient air is low due to low thermal conductivity of plastic. The module measured on the evaluation board exhibits a temperature rise of about 20°C above ambient temperature. An insufficiently cooled module will rapidly heat beyond operating range in ambient room temperature.

Packaging


(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED
REV DESCRIPTION DATE APPROVED
0 NEW DRAWING 24.10.01 MAT
MATERIAL: CONDUCTIVE POLYSTYRENE (IV)
1st Angle 3rd Angle
DRAWN: Rajesh
GENERAL TOLERANCE: ±0.2
DRAWING NO: CP216/01-0
SCALE: NTS
TITLE: OPEN TOOL EMBOSSED CARRIER TAPE DIMENSIONS BGA 2727/5
C-PAK PTE LTD
THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO C-PAK PTE.LTD.
Ao 27.59 +/- 0.1
Bo 27.59 +/- 0.1
Ko 2.72 +/- 0.1
F 20.20 +/- 0.15
P1 32.00 +/- 0.1
So 40.40 +/- 0.1
W 44.00 +/- 0.3
SECTION Y-Y

PINOUT (STM32MP2 pads named PA, PB, etc. can be used as GPIO ports)

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
1st SPI							
1	SPIA_NSS	PD5	TRACED1 **SPI4_NSS** HDP_HDP4 SAI1_D4	SAI1_FS_B - - -	TIM1_CH3N TIM4_CH2 OCTOSPIM_P1_IO1 -	- DCMIPP_D13 - -	
2	SPIA_MISO	PD4	TRACED0 **SPI4_MISO** HDP_HDP3 SAI1_D3	SAI1_SD_B - - -	TIM1_CH4N TIM4_CH1 OCTOSPIM_P1_IO0 -	- DCMIPP_D14 - -	
3	SPIA_MOSI	PD6	TRACED2 **SPI4_MOSI** HDP_HDP5 -	SAI1_SCK_B MDF1_SDI2 - -	TIM1_CH2N TIM4_CH3 OCTOSPIM_P1_IO2 -	- DCMIPP_D12 - -	
4	SPIA_SCK	PD7	DEBUG_TRACED3 **SPI4_SCK** SPI1_RDY -	SAI1_MCLK_B MDF1_CKI2 - -	TIM1_CH1N TIM4_CH4 OCTOSPIM_P1_IO3 -	- DCMIPP_D11 - -	
I2C							
5	I2CA_SCL	PF2	- - SPI3_RDY -	- - - -	TIM12_CH1 **I2C2_SCL** ETH1_MDIO ETH2_MII_COL	FMC_NE4 I3C2_SCL - -	
6	I2CA_SDA	PB4	- - SPI2_RDY UART4_CTS	SAI4_FS_B - TIM14_CH1 -	- **I2C2_SDA** OCTOSPIM_P2_IO4 -	- I3C2_SDA - -	Connected to both ports due to compatibility of the MP2xx series
		PD15	- SPI1_RDY - -	- DSIHOST_TE I2C5_SDA FDCAN1_TX	TIM1_BKIN2 TIM5_ETR I2C7_SCL FMC_D3/FMC_DA3	SDMMC3_CKIN DCMIPP_D0/DCMI_D0/PSSI_D0 - EVENTOUT	
7	INTA	**PH3**	- - I2S1_WS/SPI1_NSS -	- - UART7_RX TIM17_CH1N	- TIM5_CH3 I2C7_SCL -	- - - -	Connected to both ports due to compatibility of the MP2xx series
		PH8	- - I2S1_SDI/SPI1_MISO SPDIFRX_IN3	UART4_RX - UART7_CTS -	- TIM5_CH1 I2C3_SMBA I2C2_SMBA	- - - -	
8	I2CB_SCL	PZ1	- - LPTIM3_CH1 SPI8_MISO	TIM8_CH2 - LPUART1_RX LPTIM5_ETR	**I2C8_SCL** I2C8_SMBA - I3C4_SCL	- - - -	
9	I2CB_SDA	PZ0	- - LPTIM3_IN1 SPI8_MOSI	TIM8_CH1 - LPUART1_TX LPTIM5_OUT	**I2C8_SDA** - LPTIM3_CH2 I3C4_SDA	- - - -	
10	INTB	**PD14**	- - I2S1_MCK -	- - - FDCAN1_RX	TIM11_CH1 - I2C7_SDA FMC_D4/FMC_DA4	SDMMC3_D3 DCMIPP_D1 - -	
CAN							
11	CANA_RX	PB11	- I2S3_MCK - -	- - USART1_CTS/USART1_NSS **FDCAN1_RX**	- TIM12_CH2 OCTOSPIM_P2_NCLK OCTOSPIM_P2_NCS2	FMC_D14/FMC_DA14 OCTOSPIM_P1_NCS2 - -	
12	CANA_TX	PB9	- SPI3_RDY - -	- - USART1_DE/USART1_RTS **FDCAN1_TX**	- TIM10_CH1 OCTOSPIM_P2_DQS OCTOSPIM_P2_NCS2	FMC_D13/FMC_DA13 - - -	
13	CANB_RX	PA5	- - - SPI4_MOSI	SAI2_MCLK_B SAI2_SD_B USART2_DE/USART2_RTS **FDCAN2_RX**	TIM2_CH4 - LTDC_G0 -	FMC_A0 DCMI_D13/PSSI_D13 - -	
14	CANB_TX	PC3	- LPTIM1_IN2 I2S3_WS/SPI3_NSS -	- - USART6_DE/USART6_RTS **FDCAN2_TX**	- - ETH2_RX_CTL/CRS_DV ETH1_MII_RX_ER	- LTDC_G6 DCMI_D3/PSSI_D3 -	
SAI							
15	SAI_TX	PD1	- HDP_HDP1 I2S1_SDI/SPI1_MISO SAI1_CK2	- **SAI4_SD_A** UART7_DE/UART7_RTS TIM15_CH1	TIM1_BKIN - OCTOSPIM_P1_NCLK OCTOSPIM_P1_NCS2	OCTOSPIM_P2_NCS2 DCMIPP_HSYNC - -	

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
16	SAI_RX	PB5	- - I2S2_MCK UART4_DE/UART4_RTS	**SAI4_SD_B** - - -	- I2C2_SCL OCTOSPIM_P2_IO5 -	FMC_D8/FMC_DA8 I3C2_SCL SDMMC3_D123DIR -	
17	SAI_SCK	PD2	- HDP_HDP2 I2S1_WS/SPI1_NSS SAI1_CK1	- **SAI4_SCK_A** UART7_CTS TIM15_BKIN	TIM1_ETR - OCTOSPIM_P1_DQS OCTOSPIM_P1_NCS2	- DCMIPP_VSYNC - -	
18	SAI_FS	PD0	DEBUG_TRACECLK HDP_HDP0 - SAI1_D2	- **SAI4_FS_A** UART7_RX TIM15_CH2	- - OCTOSPIM_P1_CLK -	- DCMIPP_PIXCLK - -	
ETHERNET 1							
19	ENET_RST	**PB2**	- - I2S2_SDO/SPI2_MOSI -	- MDF1_CKI3 TIM17_BKIN TIM16_BKIN	- - OCTOSPIM_P2_IO2 -	- - - -	
20	ENET_CK125	PH9	- - - -	SAI3_MCLK_A - USART6_RX TIM15_CH1N	- - **ETH1_RGMII_CLK125** ETH1_MII_RX_ER	- - - -	ADC3_INP4
21	ENET_INT	PC6	- RTC_REFIN SPDIFRX_IN0 -	- MDF1_CKI1 - -	TIM8_CH1 - ETH2_MDC ETH1_MII_CRS	FMC_A24 **ETH1_PHY_INTN** LTDC_CLK -	ADC1_INP9, ADC1_INN5, ADC2_INP9, ADC2_INN5
22	ENET_MDIO	PA10	- - - SPI4_MISO	SAI2_SD_B - USART2_RX LPTIM5_IN1	TIM2_CH2 - **ETH1_MDIO** -	LTDC_R6 DCMIPP_D15/PSSI_D15 - -	
23	ENET_MDC	PF4	- RTC_OUT2 - -	SAI3_SCK_A - USART6_RX TIM4_CH4	**ETH1_MDC** ETH2_CLK ETH2_PPS_OUT ETH1_PPS_OUT	- LTDC_B7 - -	
24	ENET_RXC	PA14	- SPI8_NSS LPTIM2_CH2 -	SAI4_FS_B MDF1_CCK1 - -	- - **ETH1_RXC/REF_CLK** -	- - - -	
25	ENET_RX_CTL	PA11	- SPI8_SCK LPTIM2_CH1 -	SAI4_SD_B - - -	- - **ETH1_RX_CTL/CRS_DV** -	- - - -	
26	ENET_RXD0	PF1	- SPI8_MISO LPTIM2_IN2 -	SAI4_SCK_B - USART2_CK -	- - **ETH1_RXD0** -	- - - -	
27	ENET_RXD1	PC2	- SPI8_MOSI LPTIM2_IN1 -	SAI4_MCLK_B MDF1_SDI3 USART2_DE/USART2_RTS -	- - **ETH1_RXD1** -	- - - -	
28	ENET_RXD2	PH12	- - I2S3_WS/SPI3_NSS -	- - - -	TIM10_CH1 - **ETH1_RXD2** -	- - - -	
29	ENET_RXD3	PH13	- - I2S3_CK/SPI3_SCK -	- - - TIM15_BKIN	TIM11_CH1 - **ETH1_RXD3** -	- - - -	
30	ENET_TX_CTL	PA13	- SPI8_RDY I2S3_MCK LPTIM2_ETR	- MDF1_CKI3 USART2_CTS/USART2_NSS -	- I2C7_SMBA **ETH1_TX_CTL/TX_EN** -	- - - -	
31	ENET_TXC	PC0	- LPTIM1_CH1 - -	SAI3_MCLK_B USART6_TX - -	- DCMIPP_D0 ETH2_RMII_REF_CLK ETH1_MII_TX_CLK	**ETH1_RGMII_GTX_CLK** LTDC_G7 - -	
32	ENET_TXD3	PH11	- - - -	SAI3_FS_A - - TIM15_CH2	- ETH2_MDIO **ETH1_TXD3** -	- - - -	
33	ENET_TXD2	PH10	- - I2S1_CK/SPI1_SCK -	SAI3_SCK_A - - TIM15_CH1	- ETH2_MDC **ETH1_TXD2** -	- - - -	ADC3_INP8, ADC3_INN4
34	ENET_TXD1	PC1	I2S3_SDO/SPI3_MOSI	- - USART2_TX -	- I2C7_SCL **ETH1_TXD1** -	- - - -	

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
35	ENET_TXD0	PA15	I2S3_SDI/SPI3_MISO	USART2_RX	- I2C7_SDA **ETH1_TXD0** -	- - - -	
SD							
36	SD_CD	**PB3**	- - I2S2_WS/SPI2_NSS -	- MDF1_SDI3 - -	- - OCTOSPIM_P2_IO3 -	FMC_NCE3 - - -	
37	SD_D1	PE5	DEBUG_TRACED1 LPTIM2_IN2 I2S1_WS/SPI1_NSS I2S3_WS/SPI3_NSS	SAI1_FS_B - USART3_DE/USART3_RTS FDCAN1_RX	- - **SDMMC1_D1** -	- - - -	
38	SD_D0	PE4	DEBUG_TRACED0 LPTIM2_IN1 I2S1_SDO/SPI1_MOSI I2S3_SDI/SPI3_MISO	SAI1_SD_B - USART3_CTS/USART3_NSS FDCAN1_TX	- - **SDMMC1_D0** -	- - - -	
39	SD_CLK	PE3	DEBUG_TRACECLK - SPI1_RDY I2S3_CK/SPI3_SCK	SAI1_MCLK_B - USART3_TX -	TIM11_CH1 - **SDMMC1_CK** -	- - - -	
40	SD_CMD	PE2	- LPTIM2_ETR I2S1_SDI/SPI1_MISO I2S3_SDO/SPI3_MOSI	SAI1_SCK_B - - -	TIM10_CH1 - **SDMMC1_CMD** -	- - - -	
41	SD_D3	PE1	DEBUG_TRACED3 LPTIM2_CH2 I2S1_MCK I2S3_MCK	- - USART3_RX -	- - **SDMMC1_D3** -	- - - -	
42	SD_D2	PE0	DEBUG_TRACED2 LPTIM2_CH1 I2S1_CK/SPI1_SCK SPI3_RDY	- - USART3_CK -	- - **SDMMC1_D2** -	- - - -	
USB							
43	USBA_VBUS	Not connected					
44	USBA_DN	USBH_HS_DM					
45	USBA_DP	USBH_HS_DP					
46	USBB_VBUS	**PC5**	- - SPDIFRX_IN1 -	- MDF1_SDI1 - -	TIM8_CH1N I2C4_SDA ETH2_MDIO ETH1_MII_COL	FMC_A25 ETH1_PPS_OUT LTDC_DE EVENTOUT	**10K/20K voltage divider** ADC1_INP10, ADC2_INP10, ADC3_INP10, TAMP_IN6
47	USBB_DN	USB3DR_DM					
48	USBB_DP	USB3DR_DP					
POWER SUPPLY & RESET							
49 50	VIN	3.3V power supply input					
51	NRST	Open drain reset to reset of external devices, or to reset the device. Connected to STM32MP2 NRST and PCA9450 POR_B, 10K-PU					
52	BOOT_MODE	Connected to STM32MP2 BOOT1, 10K-PU. BOOT[0,2,3]=L					H: Boot from eMMC L: Boot from USB
DISPLAY							
53	LCD_DE	PI5	- - SPI5_MOSI I2S1_SDO/SPI1_MOSI	- UART5_CTS - -	TIM5_CH2 - - -	- **LTDC_DE** DCMI_D1/PSSI_D1 -	
54	LCD_VSYNC	PI6	- RCC_MCO_1 - -	- - USART3_TX TIM2_ETR	TIM3_CH1 - - -	- **LTDC_VSYNC** - -	WKUP4
55	LCD_HSYNC	PG2	- RTC_REFIN I2S3_MCK -	SAI2_FS_A - USART3_CK -	TIM5_CH3 - ETH2_MII_TX_CLK ETH2_RGMII_CLK125	FMC_CLK **LTDC_HSYNC** - -	WKUP5, ADC1_INP2, ADC2_INP2
56	LCD_CLK	PF12	DEBUG_TRACECLK - SPI5_MISO I2S1_SDI/SPI1_MISO	- - - -	TIM5_CH1 - - -	- **LTDC_CLK** DCMI_D0/PSSI_D0 -	
57	LCD_R1	PA4	- - - -	- - USART2_TX FDCAN2_TX	TIM2_CH1 - **LTDC_R1** -	- ETH1_PTP_AUX_TS - -	

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
58	LCD_R2	PC11	- LPTIM1_CH1 SPI5_NSS -	SAI2_MCLK_A UART5_DE/UART5_RTS USART3_DE/USART3_RTS TIM3_CH1	TIM5_ETR - ETH2_RXD3 -	FMC_NBL1 **LTDC_R2** DCMIPP_D10 -	ADC1_INP7, ADC1_INN3, ADC2_INP7, ADC2_INN3, ADC3_INP7, ADC3_INN3
59	LCD_R3	PA1	- - - -	SAI3_SD_A USART1_DE/USART1_RTS USART6_CK TIM4_CH2	- - - **LTDC_R3**	- DCMI_D5/PSSI_D5 - -	
60	LCD_R4	PF15	DEBUG_TRACED2 HDP_HDP2 SPI2_RDY USART6_CTS/USART6_NSS	I2S2_CK/SPI2_SCK - USART3_CK TIM2_CH2	TIM3_ETR - - -	- **LTDC_R4** - -	
61	LCD_R5	PG5	DEBUG_TRACED3 HDP_HDP3 - USART6_DE/USART6_RTS	- - - TIM2_CH3	- - - -	- **LTDC_R5** DCMIPP_PIXCLK -	
62	LCD_R6	PF3	- - - -	SAI2_SCK_B MDF1_CCK0 - TIM3_CH4	TIM8_BKIN2 ETH1_CLK ETH2_PPS_OUT -	FMC_A20 **LTDC_R6** DCMI_HSYNC/PSSI_DE -	ADC1_INP16, ADC1_INN15
63	LCD_R7	PG7	DEBUG_TRACED5 HDP_HDP5 SPI5_NSS I2S1_WS/SPI1_NSS	- - - -	TIM5_ETR - - -	- **LTDC_R7** DCMI_VSYNC/PSSI_RDY -	
64	LCD_G2	PC9	- RCC_MCO_1 I2S3_SDI/SPI3_MISO -	SAI2_SCK_A - - TIM13_CH1	TIM8_CH4N USBH_HS_OVRCUR ETH2_TXD2 USB3DR_OVRCUR	FMC_A22 **LTDC_G2** DCMIPP_D7 -	ADC1_INP8, ADC1_INN4, ADC2_INP8, ADC2_INN4
65	LCD_G3	PG9	DEBUG_TRACED7 - - -	- UART5_TX - -	TIM5_CH4 - - -	- **LTDC_G3** DCMIPP_D3/DCMI_D3/PSSI_D3 -	
66	LCD_G4	PA6	- - - SPI4_SCK	SAI2_FS_B - USART2_CK TIM13_CH1	TIM2_ETR - **LTDC_G4** -	FMC_NE1 DCMI_D12/PSSI_D12 - -	
67	LCD_G5	PG11	DEBUG_TRACED9 HDP_HDP1 - -	- - - FDCAN1_TX	TIM8_CH4 - - -	- **LTDC_G5** DCMIPP_D5 -	
68	LCD_G6	PG12	DEBUG_TRACED10 HDP_HDP2 - -	- - - FDCAN1_RX	TIM8_CH1N - - -	- **LTDC_G6** DCMI_D6/PSSI_D6 -	
69	LCD_G7	PA9	- - - SPI4_NSS	SAI2_SCK_B - USART2_CTS/USART2_NSS LPTIM5_ETR	TIM2_CH3 - ETH1_MDC -	**LTDC_G7** - DCMIPP_D14/PSSI_D14 -	
70	LCD_B1	PG14	DEBUG_TRACED12 HDP_HDP4 - -	- - USART1_TX -	TIM8_BKIN2 - - -	- **LTDC_B1** DCMI_D9/PSSI_D9 -	
71	LCD_B2	PG15	DEBUG_TRACED13 HDP_HDP5 - LPTIM1_CH2	- - USART1_RX -	TIM8_ETR - - -	- **LTDC_B2** DCMI_D10/PSSI_D10 -	
72	LCD_B3	PI0	DEBUG_TRACED14 HDP_HDP6 - LPTIM1_IN1	SAI4_MCLK_B - USART1_CK -	TIM8_BKIN - - -	- **LTDC_B3** DCMI_D11/PSSI_D11 -	
73	LCD_B4	PC7	- - - -	SAI3_SD_B - - -	TIM8_CH2N - ETH2_TXD0 ETH1_MII_TXD2	- **LTDC_B4** DCMIPP_D1 -	ADC3_INP9, ADC3_INN5
74	LCD_B5	PA7	- - AUDIOCLK -	- MDF1_CCK0 USART1_CTS/USART1_NSS TIM4_ETR	I2C2_SMBA - **LTDC_B5** -	- DCMI_D6/PSSI_D6 - -	
75	LCD_B6	PF5	- - - -	SAI3_MCLK_A - USART6_TX TIM4_CH3	ETH1_MDIO ETH1_CLK ETH2_PHY_INTN ETH1_PHY_INTN	- **LTDC_B6** - -	
76	LCD_B7	PI4	- - - LPTIM1_CH1	SAI4_FS_B - - -	TIM8_CH3 - - -	- **LTDC_B7** DCMIPP_D15/PSSI_D15 -	

Display Control

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
77	LCD_EN	**PC4**	- - - -	SAI3_FS_B - - -	- - ETH2_TX_CTL/TX_EN -	ETH1_RGMII_CLK125 LTDC_R0 - -	TAMP_IN1
78	LCD_BL	PF13	DEBUG_TRACED0 HDP_HDP0 AUDIOCLK USART6_TX	I2S2_WS/SPI2_NSS - USART3_CTS/USART3_NSS -	**TIM3_CH3** - - -	- LTDC_R2 - -	
MISC							
79	LCD_R0 CSI_CKP LVDS1_CLKP	PH4	- - - --	- - UART7_TX TIM17_BKIN	- TIM5_CH2 **LTDC_R0** USB3DR_OVRCUR	USBH_HS_OVRCUR ETH1_PTP_AUX_TS - -	BOOTFAILN
80	LCD_G0 DSI_DP3 LVDS0_TX3P	PF8	- RTC_REFIN - SAI3_SCK_B	- - USART3_RX TIM12_CH2	- ETH1_CLK ETH2_RGMII_CLK125 ETH2_MII_RX_ER	ETH2_RX_DV/CRS_DV **LTDC_G0** - -	
81	LCD_G1 DSI_DN3 LVDS0_TX3N	PC12	- LPTIM1_CH2 - -	- MDF1_CKI2 - -	TIM8_CH3 - ETH2_RXD1 ETH1_MII_RXD3	- **LTDC_G1** DCMIPP_D5/DCMI_D5/PSSI_D5 -	ADC1_INP17
82	LCD_B0	PA2	- LPTIM2_IN1 - -	- - USART1_RX -	I3C1_SDA - I2C1_SDA **LTDC_B0**	- DCMI_D3/PSSI_D3 - -	
MIPI-DSI							
83	DSI_DP1	DSIHOST_D1P					
84	DSI_DN1	DSIHOST_D1N					
85	DSI_DP0	DSIHOST_D0P					
86	DSI_DN0	DSIHOST_D0N					
87	DSI_CKP	DSIHOST_CKP					
88	DSI_CKN	DSIHOST_CKN					
UART							
89	UARTA_RXD	PB6	- - I2S2_SDI/SPI2_MISO **UART4_RX**	SAI4_SCK_B - - -	- - OCTOSPIM_P2_IO6 -	FMC_D9/FMC_DA9 - SDMMC3_D0DIR -	
90	UARTA_TXD	PH7	- - I2S1_SDO/SPI1_MOSI -	**UART4_TX** - UART7_DE/UART7_RTS TIM17_CH1	- TIM5_CH4 I2C7_SDA -	- - - -	
91	UARTB_RXD	PH5	- - - -	SAI2_FS_A - - TIM2_CH1	**UART7_RX** - LTDC_G1 USB3DR_VBUSEN	USBH_HS_VBUSEN ETH2_PTP_AUX_TS - -	WKUP2
92	UARTB_TXD	PD3	- SAI1_MCLK_A I2S2_CK/SPI2_SCK SAI1_D1	- SAI4_MCLK_A **UART7_TX** TIM15_CH1N	TIM1_BKIN2 - OCTOSPIM_P1_NCS1 -	- DCMIPP_D15/PSSI_D15 - -	
93	UARTC_RXD	PG10	DEBUG_TRACED8 HDP_HDP0 - -	- **UART5_RX** - -	TIM8_CH4N - - -	- LTDC_G4 DCMIPP_D4/PSSI_D4 -	
94	UARTC_TXD	PA0	- LPTIM1_CH2 SPI5_RDY -	SAI2_MCLK_B **UART5_TX** USART3_TX TIM3_ETR	TIM5_CH2 - ETH2_MII_RXD2 -	FMC_NL - DCMI_D9/PSSI_D9 -	WKUP1
95	UARTC_CTS	PG1	- LPTIM1_IN1 I2S3_MCK -	SAI2_SD_A **UART5_CTS** USART3_CTS/USART3_NSS -	TIM5_CH4 - ETH2_MII_RX_ER ETH2_MII_RXD3	FMC_NBL0 LTDC_VSYNC DCMIPP_D11/PSSI_D11 -	CTS/RTS **input** signal WKUP3, ADC1_INP6, ADC1_INN2, ADC2_INP6, ADC2_INN2, TAMP_IN4
96	UARTC_RTS	PG8	DEBUG_TRACED6 HDP_HDP6 SPI5_RDY SPI1_RDY	USART6_CK **UART5_DE/UART5_RTS** - -	TIM5_CH3 - - -	- LTDC_G2 DCMIPP_D2/PSSI_D2 -	RTS/CTS **output** signal
2nd SPI							
97	SPIB_NSS	PB1	- I2S3_WS/**SPI3_NSS** - -	- - - TIM16_CH1N	- - OCTOSPIM_P2_IO1 -	FMC_NCE4 - - -	

PIN	QSCOM STANDARD	MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
98	SPIB_MISO	PB10	- I2S3_SDI/**SPI3_MISO** - -	- - USART1_RX TIM17_CH1N	- - OCTOSPIM_P2_CLK -	FMC_D15/FMC_DA15 - - -	
99	SPIB_MOSI	PB8	- I2S3_SDO/**SPI3_MOSI** - -	PCIE_CLKREQN - USART1_TX TIM17_CH1	TIM20_CH4 - OCTOSPIM_P2_NCS1 -	FMC_D12/FMC_DA12 - - EVENTOUT	
100	SPIB_SCK	PF0	- - I2S3_CK/**SPI3_SCK** -	- - - FDCAN2_RX	TIM12_CH2 I2C2_SDA ETH1_MDC ETH2_MII_CRS	- I3C2_SDA - -	ADC1_INP11, ADC2_INP11, ADC3_INP11

Pins used for manufacturing and debugging – leave unconnected					
PIN	(SPM32MP2 PAD NAME)	**PIN**	(SPM32MP2 PAD NAME)	**PIN**	(SPM32MP2 PAD NAME)
C1	**JTAG_TDI** (JTDI)			C3	**JTAG_TCK** (JTCK_SWCLK)
		B2	**JTAG_TDO** (JTDO_TRACESWO)		
A1	**JTAG_TRST_B** (NJTRST)			A3	**JTAG_TMS** (JTMS_SWDIO)

Onboard peripherals wiring

USED FOR		MP2 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-14	Remarks
eMMC	CMD	PE15	- - - -	SAI1_SCK_A - - TIM15_CH1N	TIM1_CH1N - - FMC_NOE	SDMMC2_CMD - -	10K-PU
	CLK	PE14	- - - -	SAI1_MCLK_A - - TIM15_BKIN	TIM1_BKIN - - FMC_NWE	SDMMC2_CK - -	10K-PU
	DAT0	PE13	- - - -	SAI1_SD_A - - TIM15_CH1	TIM1_CH2N - - FMC_RNB	SDMMC2_D0 - -	10K-PU
	DAT1	PE11	- - - SAI4_D3	SAI1_FS_A - - TIM15_CH2	TIM1_CH3N - - FMC_A16/FMC_CLE	SDMMC2_D1 - -	
	DAT2	PE8	- SPI4_MOSI - SAI4_CK1	SAI4_MCLK_A MDF1_CKI0 - -	TIM1_CH1 - - FMC_A17/FMC_ALE	SDMMC2_D2 - -	
	DAT3	PE12	- SPI4_NSS - SAI4_CK2	SAI4_SCK_A MDF1_SDI0 USART1_RTS -	TIM1_CH2 - FMC_NE2 FMC_NCE1	SDMMC2_D3 - -	
	DAT4	PE10	- SPI4_SCK - SAI4_D1	SAI4_SD_A - USART1_CTS -	TIM1_CH3 - FMC_NE3 FMC_NCE2	SDMMC2_D4 SDMMC2_CKIN -	
	DAT5	PE9	- SPI4_MISO - SAI4_D2	SAI4_FS_A - USART1_CK -	TIM1_CH4 - - FMC_D0/FMC_DA0	SDMMC2_D5 SDMMC2_CDIR -	
	DAT6	PE6	- SPI4_RDY - -	SPDIFRX_IN2 - USART1_TX -	TIM1_ETR - - FMC_D1/FMC_DA1	SDMMC2_D6 SDMMC2_D0DIR -	
	DAT7	PE7	- - - SAI4_D4	SPDIFRX_IN3 - USART1_RX -	TIM1_CH4N - TIM14_CH1 FMC_D2/FMC_DA2	SDMMC2_D7 SDMMC2_D123DIR -	
PMIC PCA9450A	SDA	PI1	DEBUG_TRACED15 HDP_HDP7 - -	- - - -	TIM8_CH3N **I2C1_SDA** I3C1_SDA -	- LTDC_B4 DCMIPP_D8/PSSI_D8	1K-PU
	SCL	PG13	DEBUG_TRACED11 HDP_HDP3 SPI7_SCK -	- MDF1_CKI6 - -	TIM8_CH2N **I2C1_SCL** I3C1_SCL -	- LTDC_G7 DCMIPP_D7/PSSI_D7	10K-PU
	IRQ_B	PD11	DEBUG_TRACED7 - I2S1_CK/SPI1_SCK SAI1_MCLK_A	UART4_TX MDF1_CKI0 - -	TIM1_CH1 - OCTOSPIM_P1_IO7 SDMMC1_D4	SDMMC1_CKIN DCMIPP_D7/DCMI_D7/PSSI_D7 -	10K-PU
	POR_B	NRST					10K-PU
	PMIC_ON_REQ	PWR_ON					
	PMIC_STBY_REQ	PWR_LP					
	WDOG_B	PD8	DEBUG_TRACED4 SPI4_RDY I2S1_MCK SAI1_FS_A	UART4_CTS MDF1_SDI1 - -	TIM1_CH4 TIM4_ETR OCTOSPIM_P1_IO4 SDMMC1_D7	SDMMC1_D123DIR DCMIPP_D10/PSSI_D10 -	10K-PU

Electrical characteristics

Absolute maximum ratings

Parameter	Symbol	Min	Max	Remarks
Power supply	VIN	0V	3.9V	
Input voltage on USB VBUS pins	USBA_VBUS USBB_VBUS	0V	6V	
Input voltage on USB DN/DP pins	USBA_DN/DP USBB_DN/DP	0V	5.5V	
Input voltage on any other pins		0V	3.9V	
Storage temperature range	$T_{STORAGE}$	-40°C	85°C	

Operating ranges

Parameter	Symbol	Min	Max	Remarks
Power supply	VIN	3.1V	3.6V	
I/O input low level voltage	V_{IL}	-	0.3 x VIN	
I/O input high level voltage	V_{IH}	0.7 x VIN	-	
I/O output voltage	Refer to STM32MP2 datasheet, chap. Output voltage levels.			VDD=VIN=3.3V typ.
Operating temperature range	T_{AMB}	-25°C	85°C	
Processor junction temperature	T_J	-40°C	125°C	

Power supply currents

Parameter	Symbol	VIN	Current	Remarks
At U-Boot prompt	I_{UBOOT}	3.3V	195mA	All pins left unconnected
At Linux prompt	I_{LINUX}	3.3V	170mA	
Sleep	I_{SLEEP}	3.3V	6mA	
Maximum calculated	I_{MAX}	3.3V	700mA	Calculated on max. IDD's @ 80% onboard power supply efficiency.
Power supply rating	I_{SUPP}	3.3V	1A	With margin for sizing the power supply