

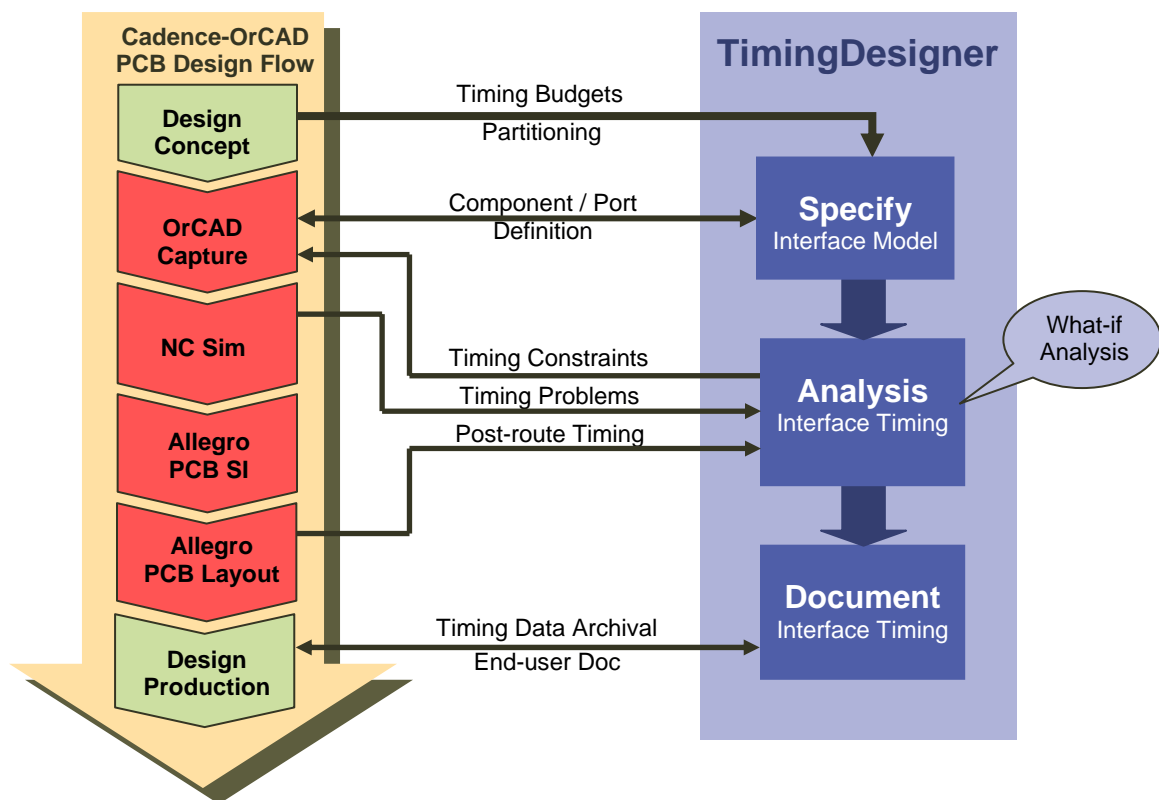
Using TimingDesigner within a Cadence/OrCAD PCB Flow

Overview:

- Built-in interface streamlines the exchange of pertinent board-level timing information between TimingDesigner and Cadence's OrCAD and Allegro design tools.
- Ability to import EDIF files from OrCAD Capture automates the creation of design components and ports for new projects within TimingDesigner, resulting in substantial time savings.
- Seamless import of net delays from Allegro PCB design tools delivers more accurate results for post-route net delay analysis and easier identification of unexpected timing closure issues.

TimingDesigner in a Cadence/OrCAD-based PCB design flow:

The diagram below illustrates how TimingDesigner is applied to a board-level design flow. It is used to specify interface timing models, perform timing analysis, and document a design's timing results for archival or end-user datasheets. Timing analysis results may be used to establish constraints for timing-driven tools, resolve timing problems from multiple sources, and confirm that post-route results have met defined timing requirements.



Design flow details:

TimingDesigner reads OrCAD-generated EDIF files to populate the *TimingDesigner manager window* with pertinent design modules that will be monitored and managed throughout the design flow.

TimingDesigner creates detailed timing constraints that are passed on to OrCAD Capture. Timing constraints are placed as properties on nets and then forwarded to downstream tools.

TimingDesigner imports VCD waveform files from NC Verilog, as well as other simulators, so timing diagrams can be created directly from simulation run data. This allows timing issues discovered during simulation to be thoroughly analyzed and provides design protocol snap-shots for product documentation material once the design project is completed.

Although TimingDesigner does not automatically read or write files directly to Allegro PCB SI formats, delay information can be inserted into TimingDesigner models. Alternatively, when net delay changes are forwarded to Allegro to drive design changes in the layout, TimingDesigner imports the final net delay report.

TimingDesigner imports Allegro net propagation delay information from a routed PCB design to create a library of net delays. Library values are referenced to accurately update signal edge relationships in timing diagrams. TimingDesigner then provides an accurate picture of the propagation delay allowed for signal protocol descriptions due to PCB trace delays.

TimingDesigner also supports an extensive list of standard exchange formats to ease the hand-off of timing information between other vendor design tools and flows. Formats include: EDIF, SDF, TDML (Timing Diagram Markup Language), as well as OLE, CSV, and others.

Summary:

Using TimingDesigner in conjunction with a Cadence/OrCAD PCB flow allows users to accurately monitor and manage timing margins throughout the design process while providing opportunities to evaluate design alternatives for tough interface timing challenges and easily exchange timing critical data between project team members along the way.

For additional product information, visit www.TimingDesigner.com.