EMA TimingDesigner®

The industry's most accurate static timing analysis

DIGITAL TIMING

What's New: TimingDesigner 9.2

This document covers a list of features that have been, added, enhanced, and/or fixed with the TimingDesigner 9.2 release.

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Table of Contents

Enhanced SDC Timing Constraints Support 4
SDC Manager 4
Clock/ Derived Clocks 5
Constraints / Measures 6
Derived Signals 6
Preview 7
Selecting an SDC Variant 8
Auto Generation of SDC using TimingDesigner Constraints 8
Generating SDC using Constraints 8
Specifying a Target Constraint 9
Calculating Constraint Values 10
Re-calculating Constraint Values 11
Exporting SDC Files 12
Enhanced Altera TimeQuest Interface 12
Creating Custom TimingDesigner Altera TCL Script 12
Altera TCL Script Export Setup 13
TCL Script Options 13
Executing TCL script in Altera QuartusII 15
Importing .tdi data into TimingDesigner Spreadsheet 16
Actel Libero Interface 17
Creating Custom TimingDesigner Actel TCL Script 17
Actel TCL Script Export Setup 17
TCL Script Options 18
Executing TCL script in Actel Libero 20
Importing Actel .tdi data into TimingDesigner Spreadsheet 21
Allegro PCB SI Interface 22
Importing Delay File 22
Template Files 23
Selecting / Filtering Data 23
Importing Options 24
Net / Pin Mapping 25
Importing Manipulating Data 25
General Usability Enhancements 26
Convert to Derived Clock 26
Converting a Clock 26
SDF Import 28
Library Browser Enhancements 28
Tree View 28
Variable Overrides 29
Library Window 30
Add Alias through Manager Window 30
New Icons 31
.TDP and .TDC icons 31
Backup file Icons 32
Over 100 New Design Kits since Version 9.1 Released 33
PCR's Fixed 34
Where to Go for Help 35
Support 35
Support Contact Information 35
General Contact Information 35

Table of Figures

Figure 1: SDC Generation Error Dialog 5
Figure 2: SDC Manager Clocks / Derived Clocks 5
Figure 3: SDC Manager Constraints / Measures 6
Figure 4: SDC Manager Derived Signals 7
Figure 5: SDC Manager Preview and Export 7
Figure 6: Generating SDC from a constraint 9
Figure 7: Defining a target constraint 10
Figure 8: Re-Calculating SDC value 11
Figure 9 - Altera TCL Export Setup 13
Figure 10 - Importing Altera Delay 16
Figure 11: Actel Tcl Export Setup 18
Figure 12: Importing Actel Delay 21
Figure 13: Cadence Allegro PCB SI Report Dialog 22
Figure 14: TD SI import dialog 23
Figure 15: TD SI import net and pin mapping 25
Figure 16: Executing Create Derived Clock Command: 27
Figure 17: Completed Derived Clock command 27
Figure 18: Updated SDF import dialog 28
Figure 19: Library Browser with tree view 29
Figure 20: Library Browser Overrides 30
Figure 21: Adding Alias through library browser 31
Figure 22 - Design Kit Page (EMA Support Site) 33

Enhanced SDC Timing Constraints Support

TimingDesigner 9.1 brought the ability to generate SDC constraints from your timing diagram. Version 9.2 expands and enhances this effort to provide better support for multiple SDC variants, SDC management, and auto-generation of constraint values based on downstream requirements.

Benefits:

- Enables users to take advantage of powerful features in the SDC constraint format without having to learn all the nuances of writing SDC
- Generating Constraints from a diagram description ensures that the SDC commands mirror the desired design intent
- TimingDesigner allows users to easily incorporate timing delays and requirements for all components in the interface, enabling a system level view of timing.
- While using TD to generate SDC constraints users are also automatically developing documentation to describe interface timing requirements

SDC Manager

TimingDesigner now includes an SDC Manager tab to help users control and review the SDC enabled objects in their diagrams. You can access the SDC Manager through *View → SDC Manager* or shortcut key 's'.

The SDC manager consists of 4 tabs: Clock/Derived Clocks, Constraints/Measures, Derived Signals, and Preview.

In all tabs you can filter to only display objects with SDC enabled. The 'SDC Gen' row provides visual feedback on the status of SDC generation for your SDC enabled objects. It will show three status indicators:

 SDC is being generated with no errors

 SDC is being generated but data is missing

 SDC cannot be generated

You can click on the yellow and red icons to bring up a detailed list of warnings and errors causing problems with SDC generation.

Example: if the  was selected for a Clock signal that was trying to generate a create_clcok command the below warning message would be presented.

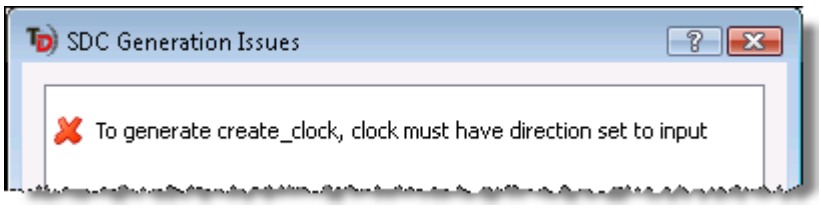


Figure 1: SDC Generation Error Dialog

The properties icon provides a link to the SDC properties screen for that particular SDC element. This provides a quick way to fix potential issues or make changes to your SDC settings.

Clock/ Derived Clocks

The clock / derived clock tab displays all the clocks and derived clocks in your diagram along with their relevant SDC information.

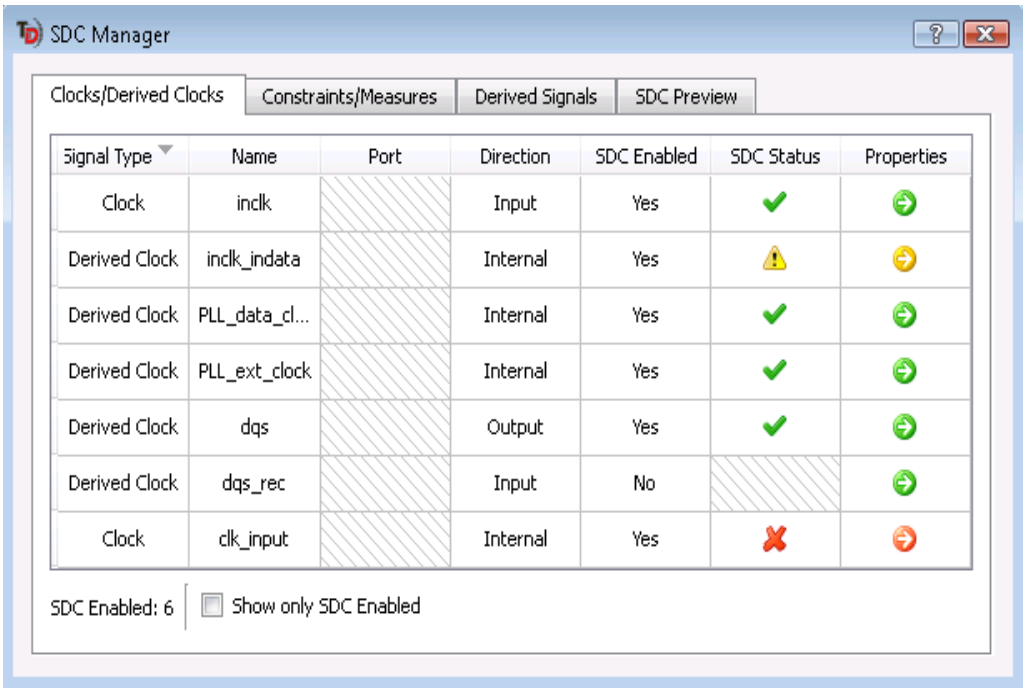


Figure 2: SDC Manager Clocks / Derived Clocks

Signal Direction and SDC (Yes/No) can be controlled form within the manager. When SDC is turned on the manager will present you with a status icon. If the yellow warning or red icon appears you can click on the icon to get a detailed description of the issue with the SDC generation.

Constraints / Measures

The constraints / measures tab displays all the constraint and measure events in your diagram along with their relevant SDC information. You can also re-calculate all the calculated SDC constraints here using the re-calc button. Calculated constraints that can be re-calculated contain an asterisk next to their value.

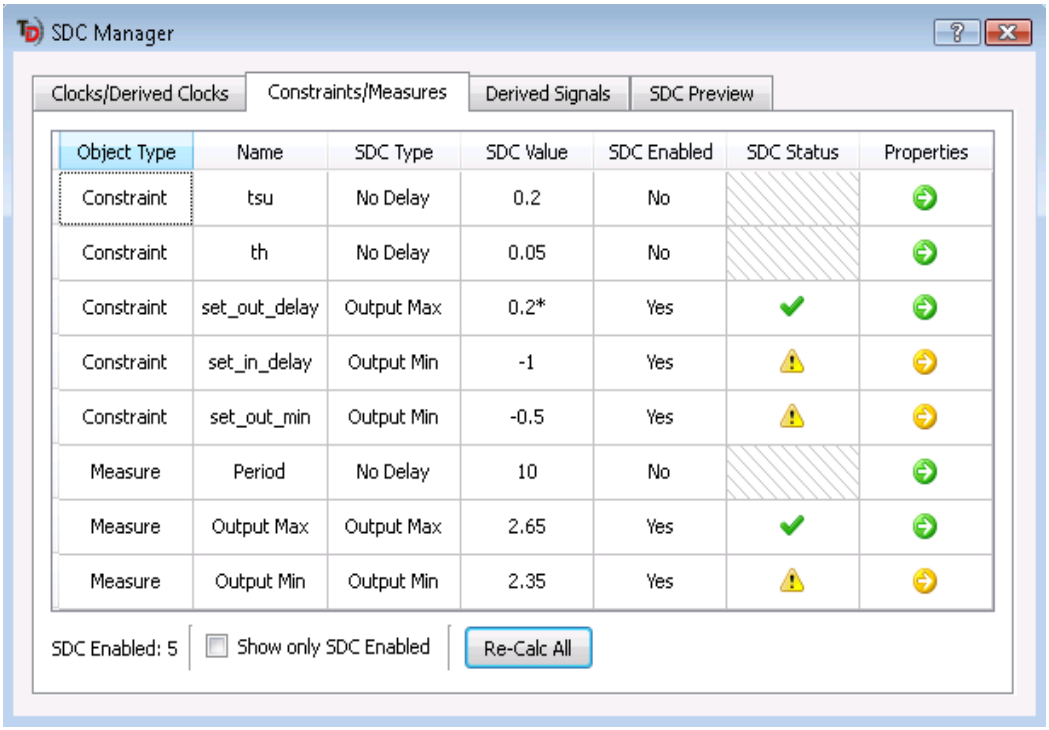


Figure 3: SDC Manager Constraints / Measures

The SDC type and SDC Enabled columns can be modified by the user. SDC type refers to the type of input/output delay you want the object in TimingDesigner to define.

The Re-Calc All button will re-calculate all the numbers presented in the SDC Value column with an asterisk next to them. This will update the value to the most current scenario presented in the diagram.

Derived Signals

The derived signals tab displays the derived signals in your design and indicates whether they are being used as SDC objects.

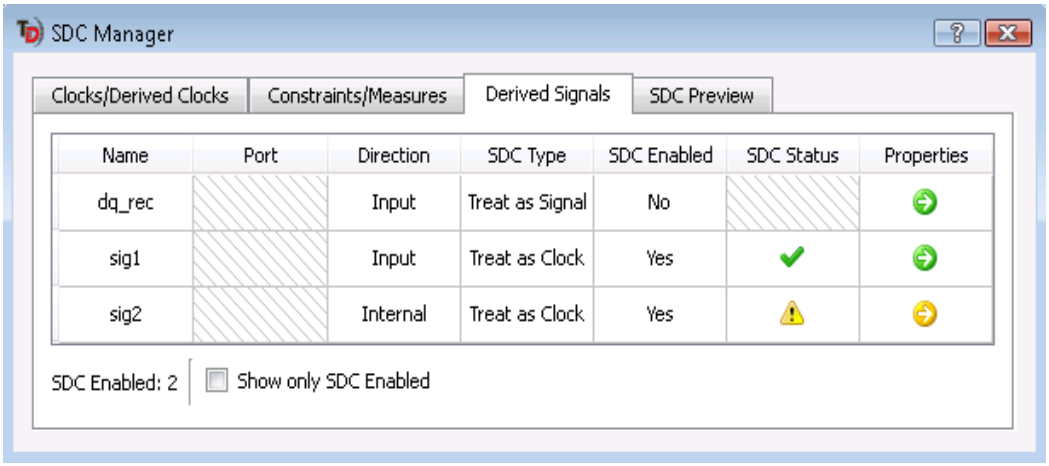


Figure 4: SDC Manager Derived Signals

Direction, SDC Type, and SDC Enabled can all be modified by the user to the desired settings.

Preview

The preview tab lets you review the SDC being generated as well as allows you to select the SDC variant you want to generate with.

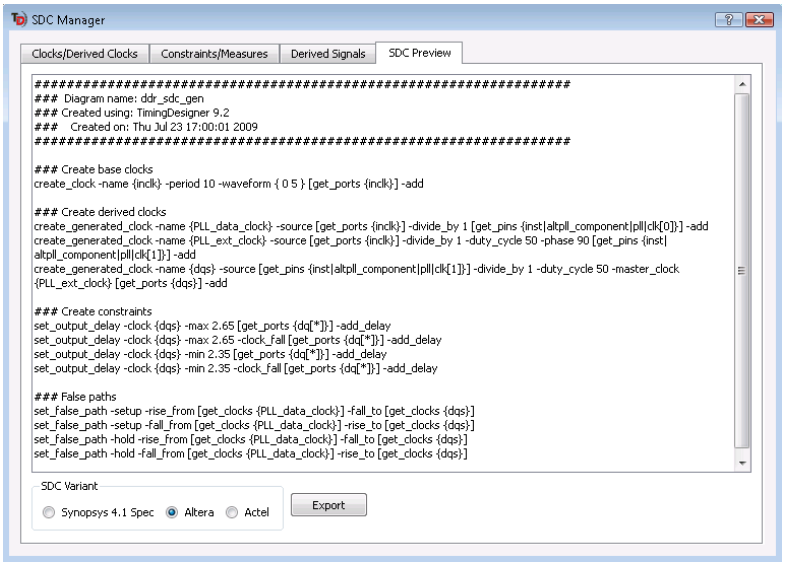


Figure 5: SDC Manager Preview and Export

Selecting an SDC Variant

Selecting a SDC Variant will ensure that SDC syntax generated only includes commands that are accepted by that particular vendor or program. You have the option to select:

- **SDC Spec:** Generates SDC conforming to the SDC 1.7 Specification.
- **Altera:** Generates SDC conforming to the Altera QuartusII SDC implementation
- **Actel:** Generates SDC conforming to the Actel Libero SDC implementation

Auto Generation of SDC using TimingDesigner Constraints

In TimingDesigner 9.1 measure objects that were used to define the position and value for both Input and Output SDC constraints. With 9.2 you can now use constraint objects along with measures to specify SDC as well as have TimingDesigner calculate what the SDC requirement is based on your diagram timing margins.

Using constraints to auto-calculate and define your SDC is especially useful for set_output_delay constraints. This is because the FPGA/IC P&R engine has a direct effect on the relative position of signals as they leave the device therefore a constraint event can be used here. The position of your output clock and data will have also have a direct affect on the setup and hold of the receiving device, so generating your constraints with those receiving device requirements in mind will help to ensure you pass timing, but be careful not to over-constrain your design.

Input delay commands typically just specify the signal relationships as they enter the device (outside the FPGA/ASIC development tools control). This input type of relationship is best suited to a measure event in TimingDesigner.

Generating SDC using Constraints

To generate SDC using a constraint, add a constraint object to the desired signal edges you want to control. Once the constraint has been added you can turn on SDC by going to the properties window, selecting the SDC tab and checking the "Generate SDC" box [Note: you can also control SDC on / off settings using the SDC manager]

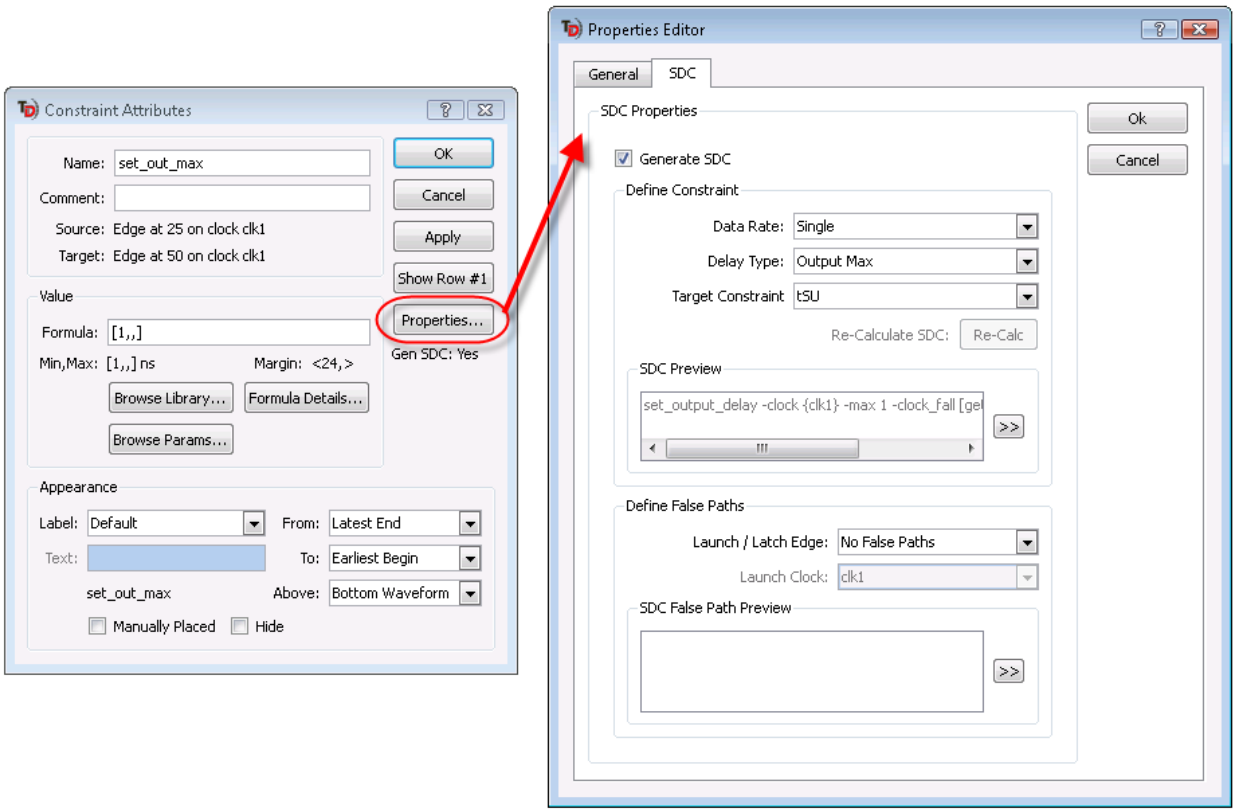


Figure 6: Generating SDC from a constraint

Once SDC has been set to generate TimingDesigner will look for the formula value in the Constraint Attributes window to determine the SDC constraint. This formula value can be added manually by the user or automatically calculated by TimingDesigner using the target constraint command in the SDC tab.

Specifying a Target Constraint

Specifying a target constraint will enable auto-calculation of SDC values. To specify the constraint select the constraint from the target constraint drop-down that you want to base your SDC value on. TimingDesigner will then use the margin of that constraint to calculate the SDC to ensure design requirements will be met. This value will be entered in the constraint formula field as well as in the SDC preview.

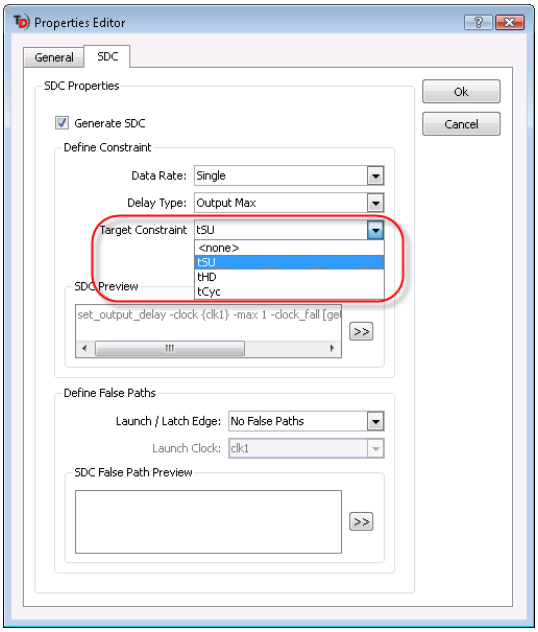


Figure 7: Defining a target constraint

To achieve proper results with this method it is assumed that the target constraint is the requirement being directly affected by the SDC value being defined. For example a setup constraint at the receiving device would be a target constraint for a set_out_max requirement at the output pins of the FPGA / ASIC.

Calculating Constraint Values

Calculated SDC uses the margins of the target constraint you defined and the current distance between the two edges of your SDC constraint (measure) to calculate the SDC requirement. TimingDesigner uses the following equations depending on the characteristics of your diagram to arrive at the SDC required value.

This is to accommodate various methods vendors use to spec their device requirements. Some define the minimum data valid window while others define the maximum data invalid window. TimingDesigner will perform the correct calculation to define SDC based on the context of the requirement (whether it's specifying valid or invalid).

1. **Target constraint has a min margin only**

   Value of SDC constraint = measure of SDC constraint (min) – margin of target constraint

2. **Target constraint has a max margin only**

   Value of SDC constraint = measure of SDC constraint (max) + margin of target constraint

3. **Target constraint has a min & max value**

Value of SDC constraint = measure of SDC constraint (max) + margin of target constraint

- When: Clock is the source and Data (not clock) is the target
  - Min constraint margin is used for Set_Output_Delay_Max calculation
  - Max constraint margin is used for Set_Output_Delay_Min calculation
- When: Clock is the target and Data (not clock) is the source
  - Min constraint margin is used for set_output_delay_min
  - Max constraint margin is used for set_output_delay_max

Re-calculating Constraint Values

As constraint margins and placement changes you may need to re-calculate SDC constraints to ensure an accurate and up-to-date representation of design requirements. Within the Constraint SDC tab a re-calc button can be used. This button will only be active when the listed value in the SDC constraint differs from the current calculated value.

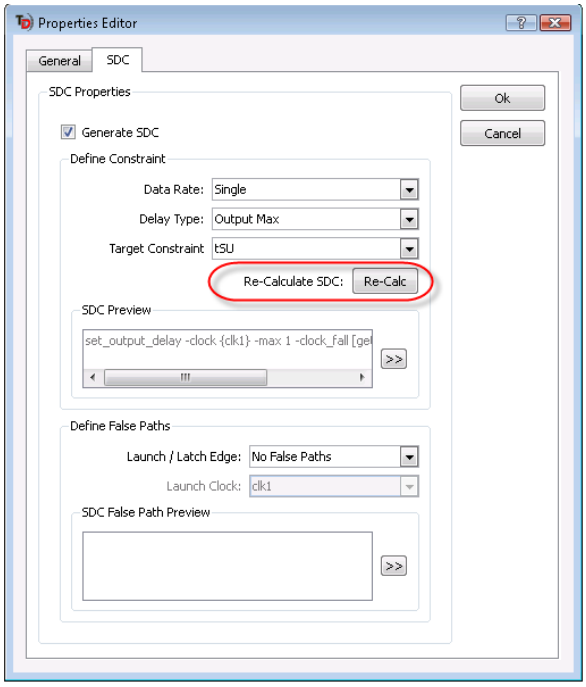


Figure 8: Re-Calculating SDC value

Pressing re-calc will then update the SDC constraint using the newly calculated value. Re-calculation is not done 'on the fly' so as to maintain synch with the FPGA/ASIC toolset. This is so users are not inadvertently evaluating place and route delays against SDC constraints that were not used to generate those P&R results.

Exporting SDC Files

Once you have defined your clock, set_input_delay, set_output_delay, and false path requirements you are now ready to export the SDC file.

To export an .SDC file from TimingDesigner go to the SDC Manager *View → SDC Manager* (shortcut key's'). Proceed to the preview tab where you can view the SDC to be generated as well as pick which variant you want to generate for.

To export the file select export and define the location you want for your file.

Tip: You can use the other tabs in the manager window as a check to make sure SDC for all the objects you are interested in are turned on and operating correctly.

For a quick export you can go to file → export and select Synopsys Design Constraint (*.sdc). You will not be presented with a preview using this method.

Enhanced Altera TimeQuest Interface

TimingDesigner 9.2 adds to and enhances the capabilities of the Altera TImeQuest Interface released in version 9.1. This new release provides support for more reporting formats as well as support for 65nm and smaller geometry devices

Alteras' TimeQuest Timing Analyzer is Altera's advanced timing environment developed for use with Synopsys Design Constraints (SDC). The TimeQuest Timing Analyzer contains a TCL scripting interface which allows users to generate custom timing reports.

TimingDesigner comes installed with an Altera TCL Script template which allows you to run custom reports in the TimeQuest tool and extract relevant timing delay data to include in your TimingDesigner projects. The TCL file collects delay information from the Altera tool based on the SDC enabled elements in your specific timing diagram.

This import capability allows the user a full design flow from generating design specifications for the Altera tool set using the TimingDesigner SDC export feature to importing post place and route timing data back into TimingDesigner for analysis and system level design validation.

The Altera TCL Script is for use with Altera Quartus versions 8.0 and above.

Creating Custom TimingDesigner Altera TCL Script

Altera TCL Scripts are generated for a specific TimingDesigner timing diagram. The script will automatically read your timing diagram and collect a list of ports for the input and output clocks with SDC enabled. It will also collect any input or output data signals that are tied to a measure event with an active set_input_delay or set_output_delay constraint. This list of

ports will define the search parameters to pull data out of the TimeQuest tool. This method reduces the overall data set and ensures you will be importing and applying timing delay data relevant to your specific timing diagram.

To export a custom Altera TCL Script file from TimingDesigner go to the diagram window, file → "export to file" and select FPGA Tcl file (*.tcl). You can then name the file and save it off to a directory of your choice. It is recommended to save the TCL file to the project directory of the Altera design you want to extract delay data from as this is where the file will need to be when running the script in Altera TimeQuest.

Once you have selected the save location for the TCL script you will then be prompted with an export setup window which will allow you to define the timing delay values to pull from the TimeQuest tool for import into TimingDesigner

Altera TCL Script Export Setup

The Altera TCL Script Export Setup allows you to define and specify the timing values you want to include in your diagram specific custom timing report. Make sure you have the Export Setup tab switched to Altera when choosing your settings.

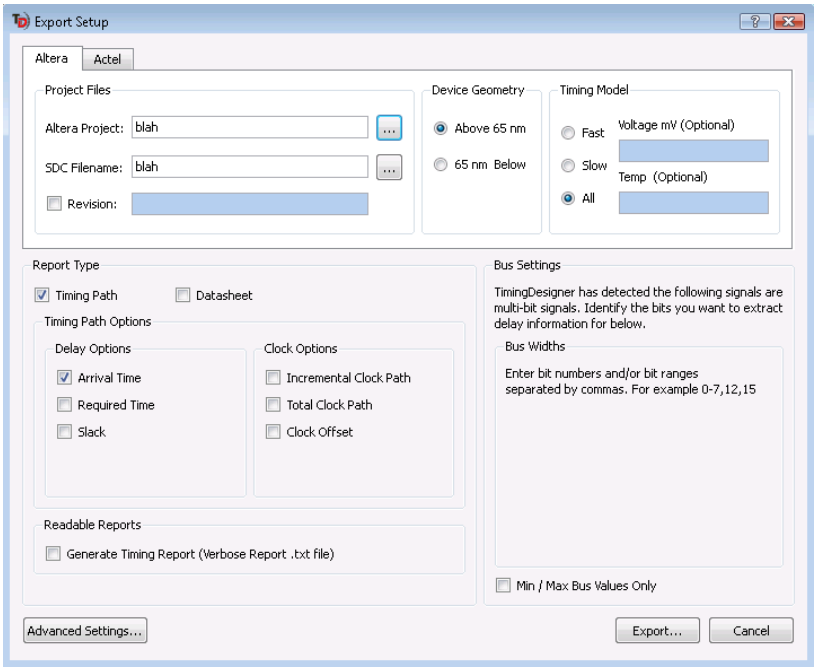


Figure 9 - Altera TCL Export Setup

TCL Script Options

- Project Files:
  - Altera Project: This is where you define the name of the Altera project you want to extract timing delays from (no file extension required). You can type the name or browse to it by clicking the browse button.

        - Revision (optional): Some Altera users specify a revision within the project. If the Altera revision mechanism is used, select the check box to enable the text field and enter the name of the revision with which the Tcl script will operate. Otherwise, deselect the revision check box,
    - SDC Filename: This is where you define the name of the SDC file used to drive timing analysis in TimeQuest (no file extension required). Typically this will be the same SDC file you generated from your TimingDesigner diagram. You can type in the name or browse to it by clicking on the browse button

- Device Geometry: Defines options for timing model selection.
    - Above 65 nm: Select here if your target device geometries are larger than 65nm (examples are Stratix II, Cyclone II)
    - 65 nm and Below: Select here if your target device geometries are 65nm or smaller (examples are Stratix III, Stratix IV)
- Timing Model
    - Fast: Generates delay timing report for the fast timing model
    - Slow: Generates delay timing report for the slow timing model
    - Both / All (65nm and below option): Generate timing reports for all valid timing models available for your device
        - Both: For above 65nm will generate fast and slow reports
        - All: For Below 65nm will generate reports for all available operating conditions
    - Voltage (65 nm and below option): Allows you to define specific Voltage conditions for timing report generation, which is required at 65nm and below.
    - Temp (65mn and below option): Allows you to define specific Temperature conditions for timing report generation
        - *Note: Voltage and Temperate both need to be defined and all are used with 65 nm and below devices.*

- Report Types: This section defines characteristics for desired TimingDesigner generated reports (TimingDesigner importable files have a .tdi extension). All other reports have a .TXT extension.

    - Datasheet: Generates datasheet style report which defines your specific FPGA implementation as an off the shelf device presenting Tsu, Th, Tco, and Tpd delays.

    - Timing Path: Generates full timing path report which defines internal delays as well as signal timings at the inputs and outputs of the device/
        - Timing Path Options
            - Delay Options:
                - Arrival Time: Returns the Arrival time (Launch Clock Delay + Data Delay) for every path of every signal in your diagram that contains an active set_ input or set_ output delay requirement on it. Arrival time also returns min/max arrival times for specified busses.

                - Required Time: Returns the required time as determined by SDC definitions for selected signals.

                - Slack: Returns the margin results as slack values, which is the difference between the Required time and the Arrival time.

- Clock Options:
  - Incremental Clock Path: Returns each incremental element of the clock path that makes up the total clock path from source to destination.
  - Total Clock Path: Returns the total clock path from source to destination.
  - Clock Offset: Reports the clock offset information relative to the design's source or input clock(s).

- Bus Settings
  - Bus Widths: Provides a list of all signals tied to SDC events that are either a bus or are derived signals with the "treat as bus" option toggled to "yes". Here the user can define bits of the bus that they want to receive timing delay values for. Users can give a range 0 – 7 or define individual bits 1,3,5.
  - Min/Max Bus Values Only: Will generate only Min/Max variable for each BUS instead of describing each individual bit and presenting a min max value. This option will examine the defined bus, determine the bit with the minimum time delay, and the bit with the maximum time delay, and then report those respective values.

- Readable Reports
  - Generate Verbose Report: Generates a detailed .txt file report that can be reviewed visually. This report is not controlled by the various reporting options listed above. It contains all elements of the timing report that is customarily reported in the GUI interface for the respective FPGA timing analysis tool.

- Advanced Settings

Executing TCL script in Altera QuartusII

After the TCL script is generated specifying the name of the desired Altera project and SDC files as well as the timing model and delay data you want to import, then place the TCL script file in the desired Altera project file directory (if you have not already done so when you specified its save location initially).

Next you can run the TCL file either through the command line interface or inside the Altera TimeQuest GUI command line console. The command to run the TCL file is:

Quartus_sta –t <TCL file name>.tcl

Once the file is run you will receive feedback from the Quartus toolset stating if the run was successful. Upon a successful execution of the TCL script the delay files you specified will now be located in the Altera project. The files that can be generated by the TCL script are:

Generate Delay Report (TD Import File .tdi

For small geometries (65nm and smaller), with TimingPath flow:

Alt2TD_TimPth_<timing model setting>_<voltaget_setting>mv_<temp_setting>c.tdi

For small geometries (65nm and smaller), with DataSheet flow:
Alt2TD_DatSht_<timing model setting>_<voltaget_setting>mv_<temp_setting>c.tdi

For larger geometries (larger than 65nm) with TimingPath flow:
Alt2TD_TimPth_<timing_model_setting>.tdi

For larger geometries (larger than 65nm) with DataSheet flow:
Alt2TD_DatSht_<timing_model_setting>.tdi

Generate Timing Report (Human Readable Format)

For small geometries (65nm and samller), with TimingPath flow:
Alt_TimPaths_<timing_model_settings>_<voltage_setting>mv_<temp_setting>c.txt

For small geometries (65nm and samller), with DataSheet flow:
Alt_DatSht_<timing_model_settings>_<voltage_setting>mv_<temp_setting>c.txt

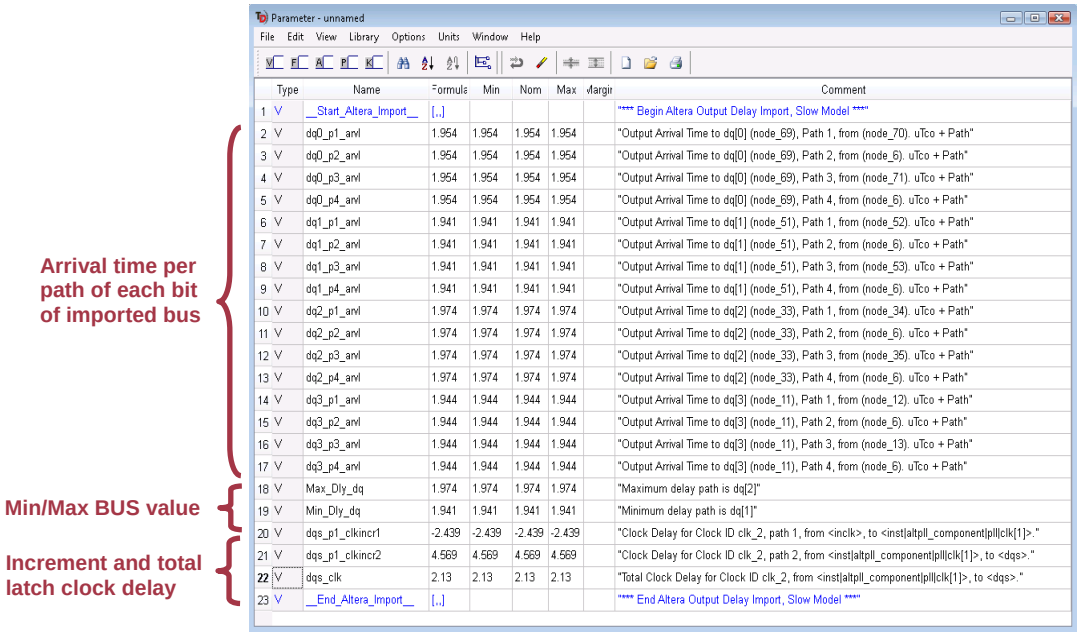
For larger geometries (larger than 65nm), with TimingPath flow:
Alt_TimPaths_<timing_model_setting>.txt

For larger geometries (larger than 65nm), with DataSheet flow:
Alt_TimPaths_<timing_model_setting>.txt

Importing .tdi data into TimingDesigner Spreadsheet

After running your custom script in Altera TimeQuest you can then import any .tdi extension files into your TimingDesigner parameter or library window.

Files can be imported in either the library or parameter window using file → Import/Merge, Altera / Actel Tcl Delay File (*.tdi) file type and browsing to the file you want to import.



	Type	Name	Formula	Min	Nom	Max	Margin	Comment
1	V	__Start_Altera_Import__	[..]					"*** Begin Altera Output Delay Import, Slow Model ***"
2	V	dq0_p1_arvl	1.954	1.954	1.954	1.954		"Output Arrival Time to dq[0] (node_69), Path 1, from (node_70). uTco + Path"
3	V	dq0_p2_arvl	1.954	1.954	1.954	1.954		"Output Arrival Time to dq[0] (node_69), Path 2, from (node_6). uTco + Path"
4	V	dq0_p3_arvl	1.954	1.954	1.954	1.954		"Output Arrival Time to dq[0] (node_69), Path 3, from (node_71). uTco + Path"
5	V	dq0_p4_arvl	1.954	1.954	1.954	1.954		"Output Arrival Time to dq[0] (node_69), Path 4, from (node_6). uTco + Path"
6	V	dq1_p1_arvl	1.941	1.941	1.941	1.941		"Output Arrival Time to dq[1] (node_51), Path 1, from (node_52). uTco + Path"
7	V	dq1_p2_arvl	1.941	1.941	1.941	1.941		"Output Arrival Time to dq[1] (node_51), Path 2, from (node_6). uTco + Path"
8	V	dq1_p3_arvl	1.941	1.941	1.941	1.941		"Output Arrival Time to dq[1] (node_51), Path 3, from (node_53). uTco + Path"
9	V	dq1_p4_arvl	1.941	1.941	1.941	1.941		"Output Arrival Time to dq[1] (node_51), Path 4, from (node_6). uTco + Path"
10	V	dq2_p1_arvl	1.974	1.974	1.974	1.974		"Output Arrival Time to dq[2] (node_33), Path 1, from (node_34). uTco + Path"
11	V	dq2_p2_arvl	1.974	1.974	1.974	1.974		"Output Arrival Time to dq[2] (node_33), Path 2, from (node_6). uTco + Path"
12	V	dq2_p3_arvl	1.974	1.974	1.974	1.974		"Output Arrival Time to dq[2] (node_33), Path 3, from (node_35). uTco + Path"
13	V	dq2_p4_arvl	1.974	1.974	1.974	1.974		"Output Arrival Time to dq[2] (node_33), Path 4, from (node_6). uTco + Path"
14	V	dq3_p1_arvl	1.944	1.944	1.944	1.944		"Output Arrival Time to dq[3] (node_11), Path 1, from (node_12). uTco + Path"
15	V	dq3_p2_arvl	1.944	1.944	1.944	1.944		"Output Arrival Time to dq[3] (node_11), Path 2, from (node_6). uTco + Path"
16	V	dq3_p3_arvl	1.944	1.944	1.944	1.944		"Output Arrival Time to dq[3] (node_11), Path 3, from (node_13). uTco + Path"
17	V	dq3_p4_arvl	1.944	1.944	1.944	1.944		"Output Arrival Time to dq[3] (node_11), Path 4, from (node_6). uTco + Path"
18	V	Max_Dly_dq	1.974	1.974	1.974	1.974		"Maximum delay path is dq[2]"
19	V	Min_Dly_dq	1.941	1.941	1.941	1.941		"Minimum delay path is dq[1]"
20	V	dqs_p1_clkincr1	-2.439	-2.439	-2.439	-2.439		"Clock Delay for Clock ID clk_2, path 1, from <inclk>, to <inst|altpll_component|pll|clk[1]>."
21	V	dqs_p1_clkincr2	4.569	4.569	4.569	4.569		"Clock Delay for Clock ID clk_2, path 2, from <inst|altpll_component|pll|clk[1]>, to <dqs>."
22	V	dqs_clk	2.13	2.13	2.13	2.13		"Total Clock Delay for Clock ID clk_2, from <inst|altpll_component|pll|clk[1]>, to <dqs>."
23	V	__End_Altera_Import__	[..]					"*** End Altera Output Delay Import, Slow Model ***"

Figure 10 - Importing Altera Delay

Figure 9 Shows example of timing delay values imported from AltTD_Import_Slow.tdi file

Subsequent import iterations of the same variables will result in an update of the variable values in the timing spreadsheet.

**Note: The Altera TCL Script template is located in the 'lib' folder of the TimingDesigner install directory. It is not a locked file and can be modified but it is recommended to make a backup copy if you intend to alter the template.*

Actel Libero Interface

Libero is Actels FPGA development environment which includes support for Synopsys Design Constraints (SDC). The Libero environment contains a TCL scripting interface which allows users to generate custom timing reports.

TimingDesigner is packaged with an Actel TCL Script template which allows you to run custom reports in the Libero tool and extract relevant timing delay data to include in your TimingDesigner projects. The TCL file collects delay information from the Actel tool based on the SDC enabled elements in your specific timing diagram.

This import capability allows the user a full design flow from generating design specifications for the Actel tool set using the TimingDesigner SDC export feature to importing post place and route timing data back into TimingDesigner for analysis and system level design validation.

Creating Custom TimingDesigner Actel TCL Script

Actel TCL Scripts are generated for a specific TimingDesigner timing diagram. The script will automatically read your timing diagram and collect a list of ports for the input and output clocks with SDC enabled. It will also collect any input or output data signals that are tied to a measure event with an active set_input_delay or set_output_delay constraint. This list of ports will define the search parameters to pull data out of the Libero tool. This method reduces the overall data set and ensures you will be importing and applying timing delay data relevant to your specific timing diagram.

To export a custom Actel TCL Script file from TimingDesigner go to the diagram window, file → "export to file" and select FPGA TCL File (*.tcl). You can then name the file and save it off to a directory of your choice. It is recommended to save the TCL file to the project directory of the Actel design you want to extract delay data from as this is where the file will need to be when running the script in Actel Libero.

Once you have selected the save location for the TCL script you will then be prompted with an export setup window which will allow you to define the timing delay values to pull from the Libero tool for import into TimingDesigner

Actel TCL Script Export Setup

The Actel TCL Script Export Setup allows you to define and specify the timing values you want to include in your diagram specific custom timing report. Make sure you have the Export Setup tab switched to Actel when choosing your settings.

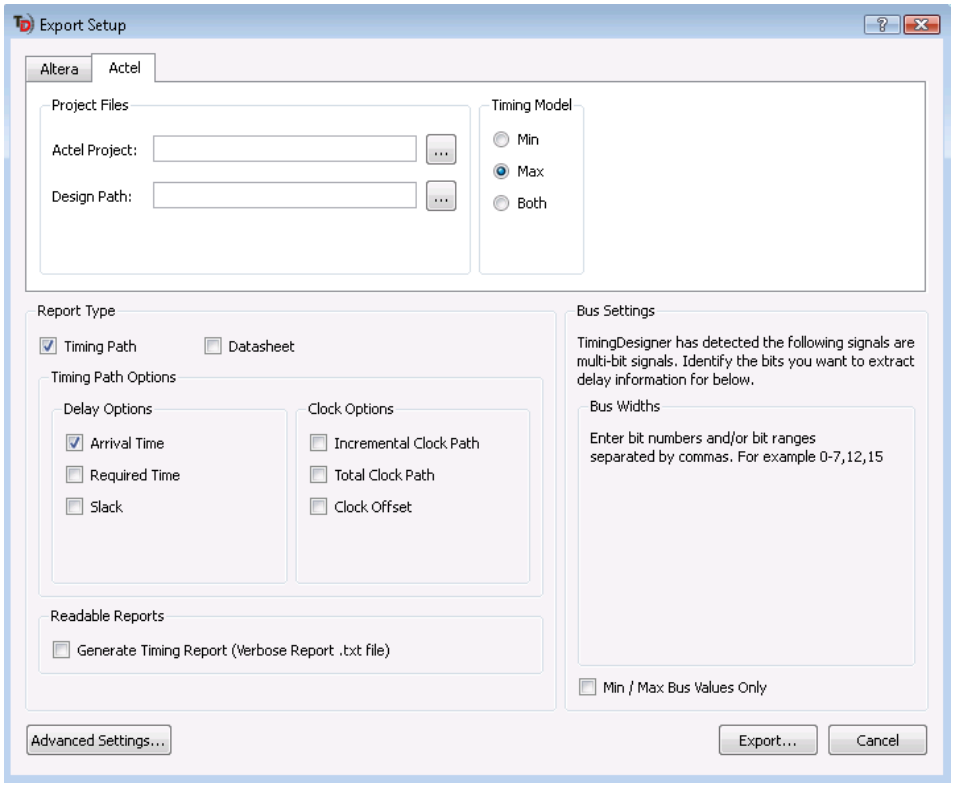


Figure 11: Actel Tcl Export Setup

TCL Script Options

- Project Files:
  - Actel Project: This is where you define the name of the Actel project you want to extract timing delays from (no file extension required). You can type the name or browse to it by clicking the browse button.
  - Design Name: This is the name of the design file for which Actel will generate in it's Designer tool with an '.adb' file extension.
  - Design Path: This is the path to the above referenced design file. Typically set to *designer\impl1* as the default Designer directory path.
- Timing Model
  - Min: Generates delay timing report for the min timing model
  - Max: Generates delay timing report for the Max timing model
  - Both: Generates timing reports one for min and max
- Report Type: This section defines characteristics for desired TimingDesigner generated reports (TimingDesigner importable files have a .tdi extension). All other reports have a .TXT extension.

- Datasheet: Generates datasheet style report which defines your specific FPGA implementation as an off the shelf device presenting Tco delays and setup and hold constraints.

- Timing Path: Generates full timing path report which defines internal delays as well as signal timings at the inputs and outputs of the device.

    - Timing Path Options
        - Delay Options:
            - Arrival Time: Returns the Arrival time (Launch Clock Delay + Data Delay) for every path of every signal in your diagram that contains an active set_ input or set_ output delay requirement on it. Arrival time also returns min/max arrival times for specified busses.

            - Required Time: Returns the required time as determined by SDC definitions for selected signals

            - Slack: Returns the margin result as slack values, which is the difference between the Required time and the Arrival time.

        - Clock Options:
            - Incremental Clock Path: Returns each incremental element of the clock path that makes up the total clock path from source to destination.

            - Total Clock Path: Returns the total clock path from source to destination.

            - Clock Offset: Reports the clock offset information relative to the design's source or input clock(s).

- Bus Settings
    - Bus Widths: Provides a list of all signals tied to SDC events that are either a bus or are derived signals with the "treat as bus" option toggled to "yes". Here the user can define bits of the bus that they want to receive timing delay values for. Users can give a range 0 – 7 or define individual bits 1,3,5.

    - Min/Max Bus Values Only: Will generate only Min/Max variable for each BUS instead of describing each individual bit and presenting a min max value. This option will examine the defined bus, determine the bit with the minimum time delay, and the bit with the maximum time delay, then report those respective values.

- Readable Reports
    - Generate Verbose Report: Generates a detailed .txt file report that can be reviewed visually. This report is not controlled by the various reporting options listed above. It contains all elements of the timing report that is customarily reported in the GUI interface for the respective FPGA timing analysis tool.

- Advanced Settings

Executing TCL script in Actel Libero

After the TCL script is generated place the TCL script file in the desired Actel project file directory (if you have not already done so when you specified the save location initially).

Next you can run the TCL file either through the command line interface or inside the Actel Libero GUI command line console. The command to run the TCL file through command line is:

< Install_Path>\Designer\bin\designer SCRIPT:<script_name>.tcl LOGFILE:DesignerOutput.log

Note: you must be in your Actel project directory when running this script for it to operate properly

For Example: if my Actel project directory was *C:\andrewd\ddrxproj\actel\ddrxproj* and my install path was c:\actel\designer\bin\designer

You would first go to the project directory then implement the Tcl command described above:

C:\andrewd\ddrxproj\actel\ddrxproj> *c:\actel\designer\bin\designer* SCRIPT:<script_name.tcl> LOGFILE: DesignerOutput.log

Bold Section: Your project directory
Italic Section: Actel Designer install path

Once the file is run you can look in the log file "DesignerOutput.log" file stating if the run was successful. Upon a successful execution of the TCL script the delay files you specified will now be located in the Actel project folder. The files that can be generated by the TCL script are:

Generate Delay Report (TD Import File .tdi)

For TimingPath flow:
Act2TD_TimPth_<timing model setting>.tdi

For DataSheet flow:
Act2TD_DatSht_<timing model setting>.tdi

Generate Timing Report (Human Readable Format)

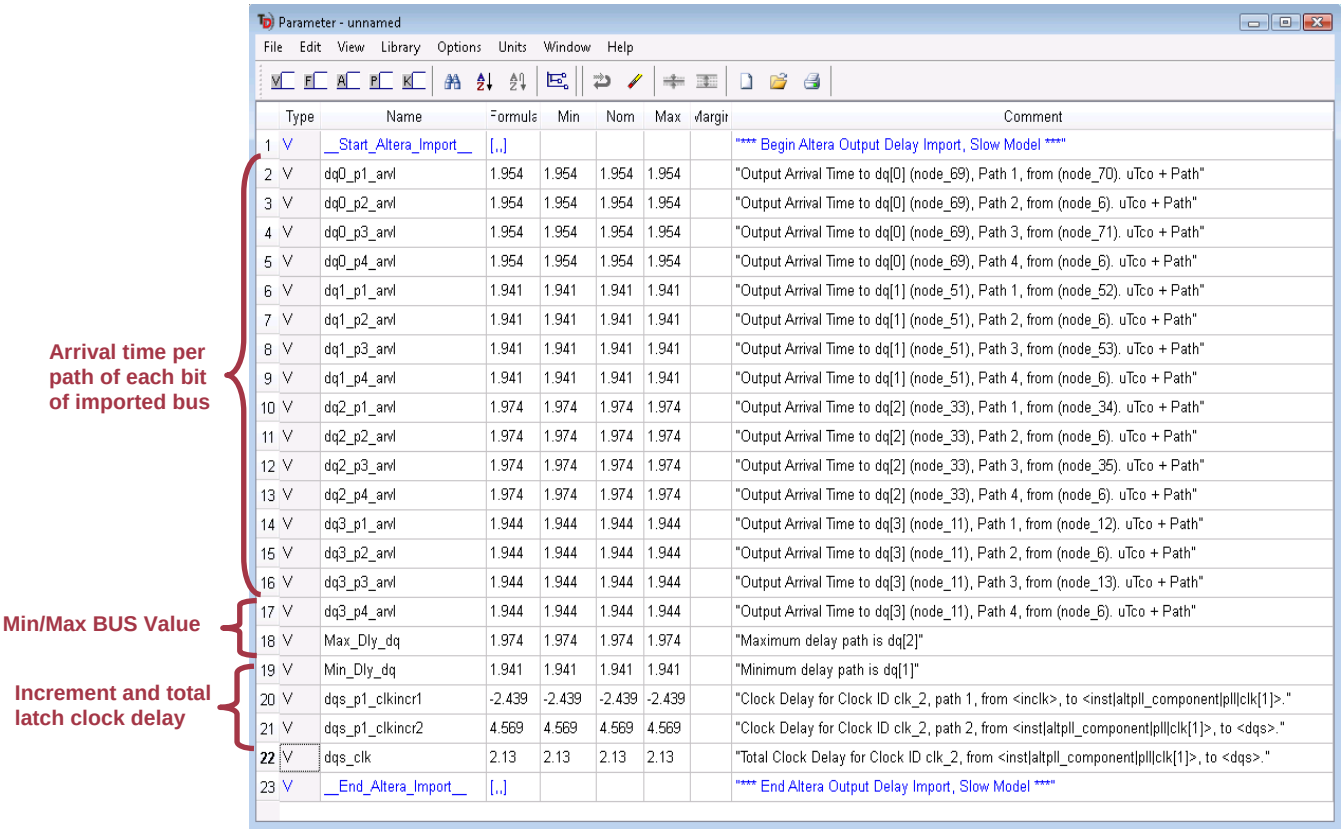
For TimingPath flow:
Act2TD_TimPth_<timing model setting>.txt

For DataSheet flow:
Act2TD_DatSht_<timing model setting>.txt

Importing Actel .tdi data into TimingDesigner Spreadsheet

After running your custom script in Actel Libero you can then import any .tdi extension files into your TimingDesigner parameter or library window.

Files can be imported in either the library or parameter window using file → Import/Merge, Altera / Actel Tcl Delay File (*.tdi) file type and browsing to the file you want to import.



	Type	Name	Formula	Min	Nom	Max	Margin	Comment
1	V	__Start_Altera_Import__	[,,]					"*** Begin Altera Output Delay Import, Slow Model ***"
2	V	dq0_p1_arvl	1.954	1.954	1.954	1.954		"Output Arrival Time to dq[0] (node_69), Path 1, from (node_70). uTco + Path"
3	V	dq0_p2_arvl	1.954	1.954	1.954	1.954		"Output Arrival Time to dq[0] (node_69), Path 2, from (node_6). uTco + Path"
4	V	dq0_p3_arvl	1.954	1.954	1.954	1.954		"Output Arrival Time to dq[0] (node_69), Path 3, from (node_71). uTco + Path"
5	V	dq0_p4_arvl	1.954	1.954	1.954	1.954		"Output Arrival Time to dq[0] (node_69), Path 4, from (node_6). uTco + Path"
6	V	dq1_p1_arvl	1.941	1.941	1.941	1.941		"Output Arrival Time to dq[1] (node_51), Path 1, from (node_52). uTco + Path"
7	V	dq1_p2_arvl	1.941	1.941	1.941	1.941		"Output Arrival Time to dq[1] (node_51), Path 2, from (node_6). uTco + Path"
8	V	dq1_p3_arvl	1.941	1.941	1.941	1.941		"Output Arrival Time to dq[1] (node_51), Path 3, from (node_53). uTco + Path"
9	V	dq1_p4_arvl	1.941	1.941	1.941	1.941		"Output Arrival Time to dq[1] (node_51), Path 4, from (node_6). uTco + Path"
10	V	dq2_p1_arvl	1.974	1.974	1.974	1.974		"Output Arrival Time to dq[2] (node_33), Path 1, from (node_34). uTco + Path"
11	V	dq2_p2_arvl	1.974	1.974	1.974	1.974		"Output Arrival Time to dq[2] (node_33), Path 2, from (node_6). uTco + Path"
12	V	dq2_p3_arvl	1.974	1.974	1.974	1.974		"Output Arrival Time to dq[2] (node_33), Path 3, from (node_35). uTco + Path"
13	V	dq2_p4_arvl	1.974	1.974	1.974	1.974		"Output Arrival Time to dq[2] (node_33), Path 4, from (node_6). uTco + Path"
14	V	dq3_p1_arvl	1.944	1.944	1.944	1.944		"Output Arrival Time to dq[3] (node_11), Path 1, from (node_12). uTco + Path"
15	V	dq3_p2_arvl	1.944	1.944	1.944	1.944		"Output Arrival Time to dq[3] (node_11), Path 2, from (node_6). uTco + Path"
16	V	dq3_p3_arvl	1.944	1.944	1.944	1.944		"Output Arrival Time to dq[3] (node_11), Path 3, from (node_13). uTco + Path"
17	V	dq3_p4_arvl	1.944	1.944	1.944	1.944		"Output Arrival Time to dq[3] (node_11), Path 4, from (node_6). uTco + Path"
18	V	Max_Dly_dq	1.974	1.974	1.974	1.974		"Maximum delay path is dq[2]"
19	V	Min_Dly_dq	1.941	1.941	1.941	1.941		"Minimum delay path is dq[1]"
20	V	dqs_p1_clkincr1	-2.439	-2.439	-2.439	-2.439		"Clock Delay for Clock ID clk_2, path 1, from <inclk>, to <inst|altpll_component|pll|clk[1]>."
21	V	dqs_p1_clkincr2	4.569	4.569	4.569	4.569		"Clock Delay for Clock ID clk_2, path 2, from <inst|altpll_component|pll|clk[1]>, to <dqs>."
22	V	dqs_clk	2.13	2.13	2.13	2.13		"Total Clock Delay for Clock ID clk_2, from <inst|altpll_component|pll|clk[1]>, to <dqs>."
23	V	__End_Altera_Import__	[,,]					"*** End Altera Output Delay Import, Slow Model ***"

Figure 12: Importing Actel Delay

Allegro PCB SI Interface

TimingDesigner 9.2 provides an interface with Cadence Allegro PCB SI to aid in more accurate timing analysis.

Joint SI and Timing analysis is becoming increasingly important as design speeds go up, margins shrink, and project schedules get shorter. Allowing users to import simulated interconnect delays from Cadence Allegro PCB SI enables design teams to resolve timing accurately and early in the design process.

Importing Delay File

TimingDesigner imports a standard delay file generated from the Allegro PCB SI tool. You can generate this report file by going to *Analyze → Reports* within the Allegro PCB SI tool and selecting the "delay report" option

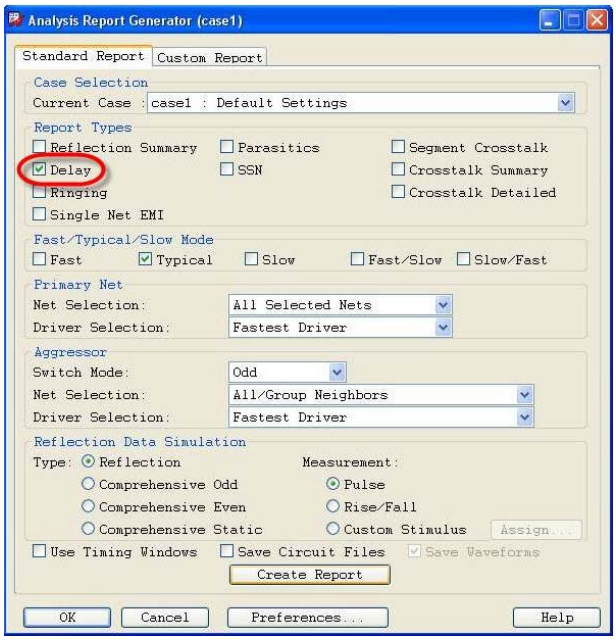


Figure 13: Cadence Allegro PCB SI Report Dialog

To import the delay file select *File → Import/Merge* from either the Parameter Spreadsheet or the Library Window. Select *Allegro PCB SI Delay File* from the file type pull down then select the file to import and click "Open". The TD SI Import Window will appear:

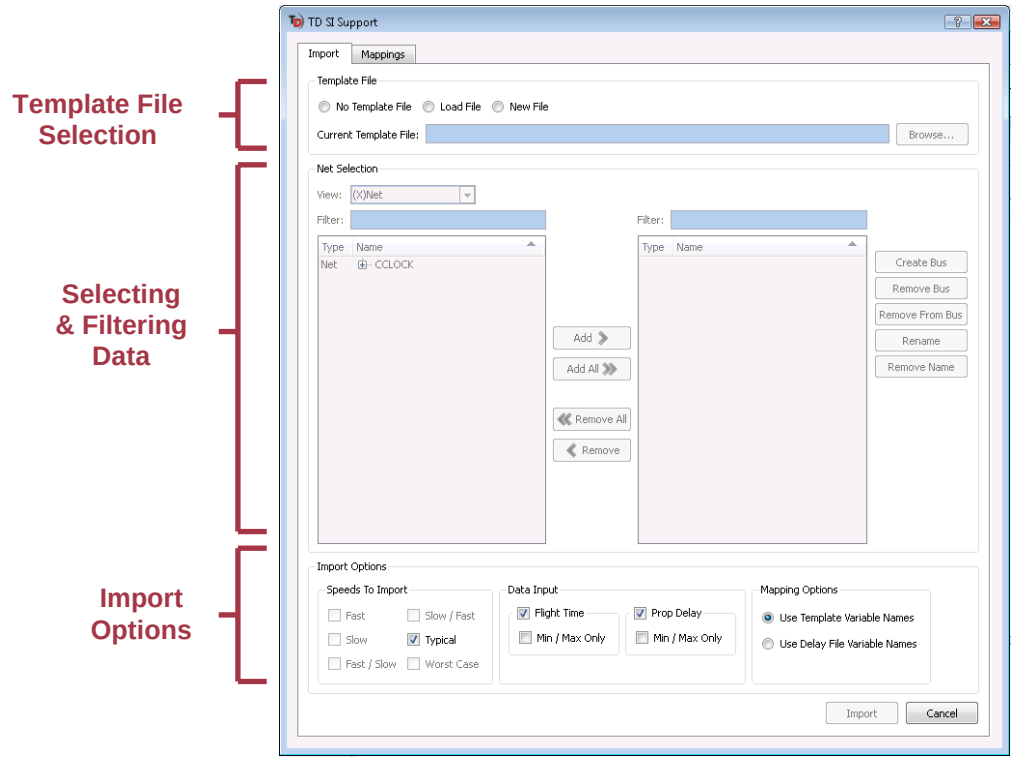


Figure 14: TD SI import dialog

Template Files

The Template file is used to store net selections, renames, and BUS groupings you have made previously to facilitate subsequent imports of SI delay data. These template files are saved with the .tf extension and are generated in XML.

Template files will also store the date stamp of your Allegro PCB SI report file and warn you if you try to use a template with a delay file older than the last used.

You can select

No Template File: No template file is used for this import session

Load File: Browse to a template file to apply to your current Allegro PCB SI Delay file

New File: Name and Save a new template file to be generated upon import.

Selecting / Filtering Data

This is the main area to select, group, and rename your nets for import into TimingDesigner. The section provides multiple views of your imported data so you can see the data as a list of:

Devices
Reference Designators

Driver Receiver Pairs
(X) Nets

Each view is tied to the other so if you add a pair of devices in the device view it will add the corresponding reference designators, drivers and receivers, and (X)nets. Objects listed in grey indicate that part of the object is being added (Example: some nets of the device pair are being added but not all).

At the net level you also have the option to view all the Pin Pair connections for that corresponding net and can add all the Pin Pairs for that net or choose specific ones.

The right dialog represents the nets you have chosen to be imported into TimingDesigner. You can rename nets and devices and group nets into Buses. By grouping nets into Buses TD will then automatically create variables that sum the min and max values of that BUS for the user.

In the case of large import files the user can also filter the left and right lists independently to help find items of interest.

Importing Options

Here you can select the different FST Modes / Delay Types to Import.

Speeds to Import:

Fast
Typical
Slow
Fast / Slow
Slow / Fast
Worst Case*

The speeds available to you are based on the FST Modes selected when the delay report was generated in Allegro PCB SI.

*The Worst Case option is calculated by TimingDesigner taking the Fast Mode Switch time and Slow Mode Settle time. This option is only available if both the Fast and Slow modes are available in the delay report.

Data Input:

Here you can elect to import Flight Time, Propagation Delay, or both. You also have the option to just import Min/Max Values only which reduces the number of variables created.

By Default TimingDesigner will generate rising, falling, and rise/fall values for the flight time of each net and a MinMax value for each BUS.

Mapping Options:

Mapping options pertains to variable naming preferences when using pin/net mapping to keep TimingDesigner synched with Allegro database changes [see net / pin mapping for more details]

Net / Pin Mapping

Upon subsequent SI delay imports pin pairs and net names may have changed. The mapping tab allows the user to make sure the delays being used in TimingDesigner are in synch with the Allegro database.

TimingDesigner will do this by comparing the nets and pin pairs in your template file with the net and pin pairs in the Allegro PCB SI delay file. Where it cannot find matches it will present these in the mapping tab to be resolved.

The user can then map to the new net names / pin pairs saving these new associations to the template file upon import.

The mapping options box lets the user decide if they want to update the current variable value but keep the name or to update the name of the variable to reflect the new net / pin assignment as well as the value.

[note: updating the variable name may require the user to update the links to that variable in their diagrams]

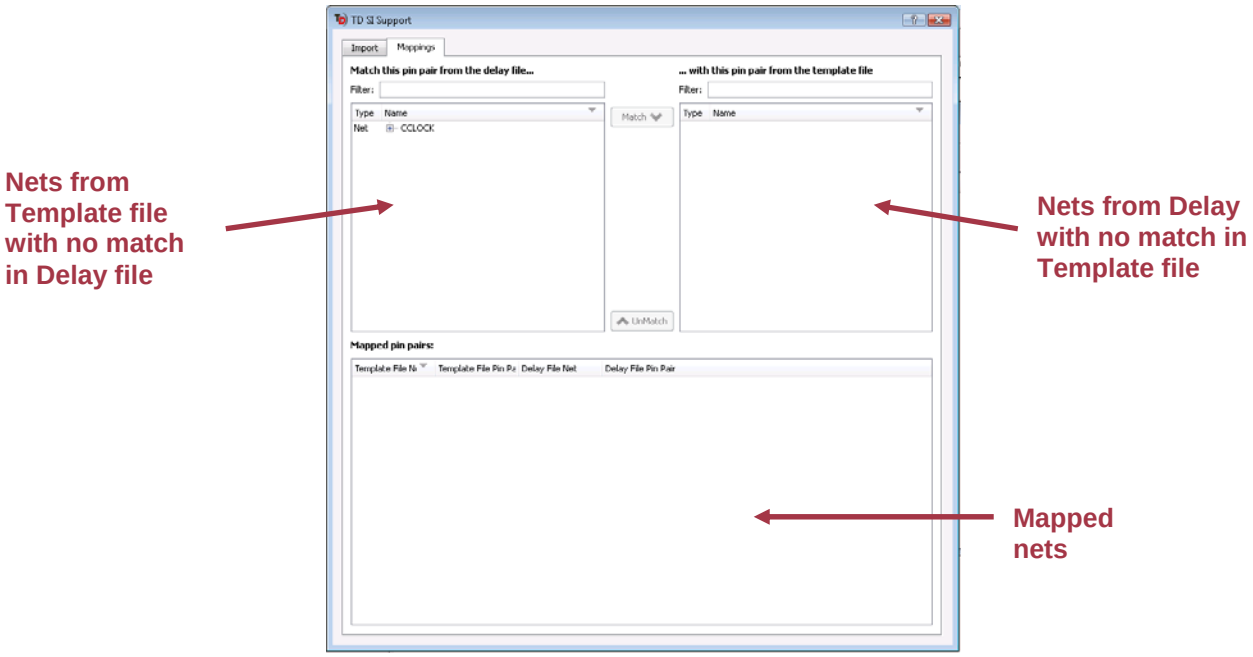


Figure 15: TD SI import net and pin mapping

Importing Manipulating Data

Once you have selected, renamed, and grouped the nets you want to import, select your import options and click Import.

If you have elected to use a template file or create a new template file TimingDesigner will ask if you want to save / update the template with your current settings. The variables TimingDesigner generates are geared to be easily searchable using the library browser. They are also built to be used with aliasing to toggle between bits in a bus for example.

Once the values are imported into TimingDesigner you can then reference them into your diagram for analysis. Subsequent Imports / Updates to these variables will be automatically applied to any diagram where these variables are used.

Tip: Unless you are importing a small amount of data it is recommended that you import the delay file into a library to utilize the hierarchical search capabilities of the library browser. This also makes it easier to reference the delay data among multiple diagrams if need be.

General Usability Enhancements

Below is a description of general changes and enhancements to the TimingDesigner software and user interface.

Convert to Derived Clock

Convert to derived clock allows the user to take a clock already present in the design and convert it to a derived clock with a new source picked from a list of clocks in the diagram. This new derived clock will collect characteristics from the original clock and pass them to the new derived clock. Characteristics passed are:

- Name
- Direction
- Port
- Objects (constraints, delays, measures, text annotations etc)

This option makes it easy for users to "connect the clocks" when merging diagrams for analysis or just providing a way to add delay to a clock using the derived clocks prop delay fields.

Converting a Clock

1. Select clock (can be a clock or derived clock) in diagram to be converted
2. Either

   a. Right Mouse Button → Convert to Derived Clock → Select Reference Clock

   b. Menu bar Tools → Convert to Derived Clock → Select Reference Clock

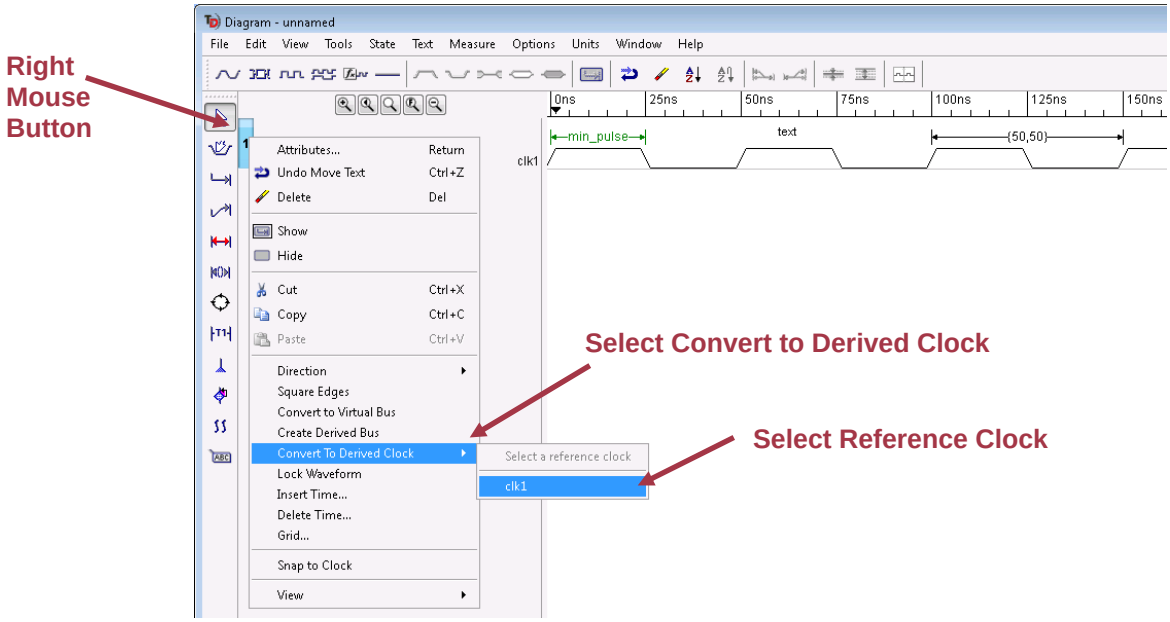


Figure 16: Executing Create Derived Clock Command:

A new Derived Clock will be generated pulling the objects and characteristics from the base clock as described above.

If the source selected was the clock itself the original clock will be renamed to _old and hidden, otherwise the clock will be deleted.

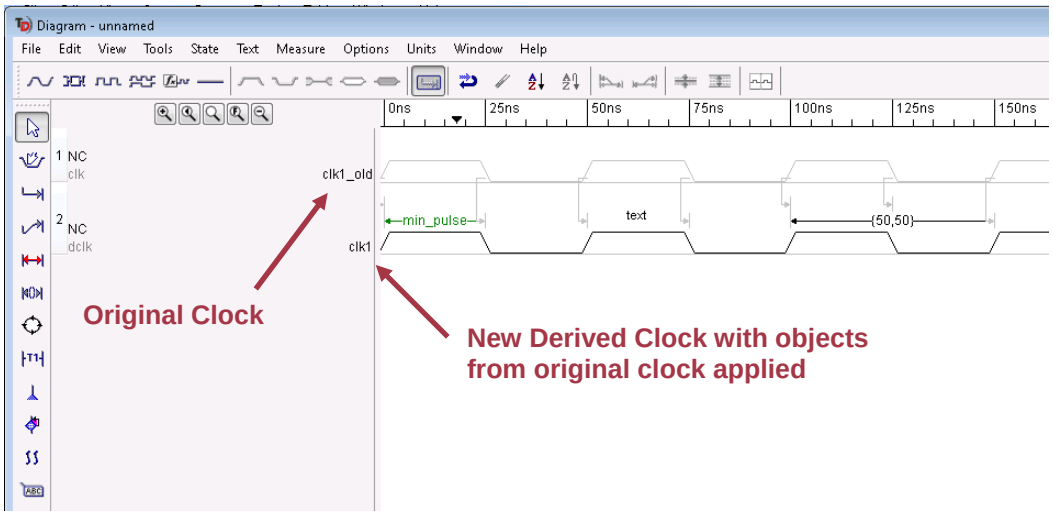


Figure 17: Completed Derived Clock command

SDF Import

SDF Import has been upgraded to present delays in a hierarchical tree format and allow selection of multiple values at once for import. Users can also now sort the SDF file contents to better find and select similar elements.

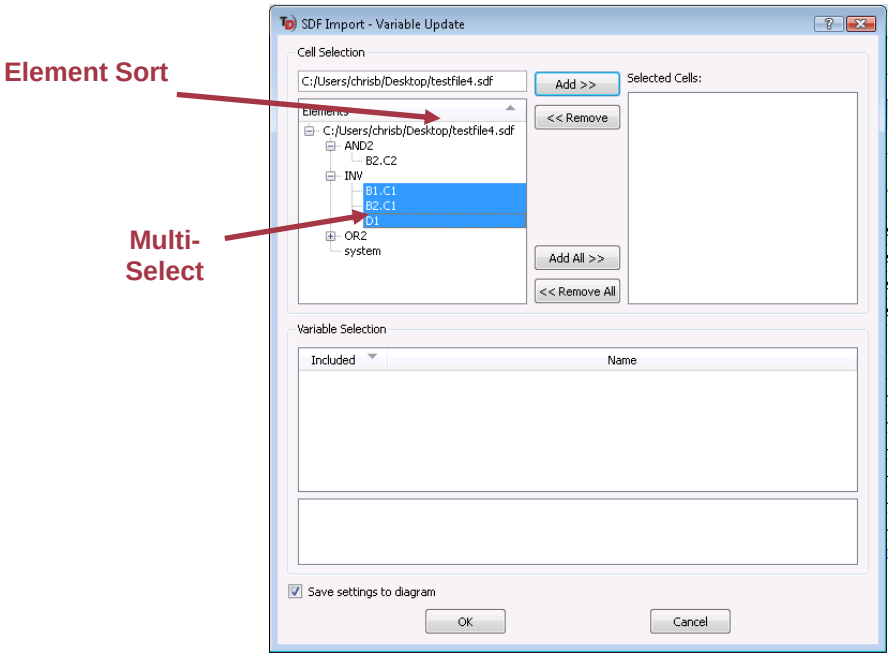


Figure 18: Updated SDF import dialog

Library Browser Enhancements

The library browser has been enhanced with a more Windows like operation to provide better ease of use.

Tree View

The TimingDesigner library browser now supports a more modern tree view. This enables clearer and easier searching for desired variables. It also helps users understand the hierarchy present in TimingDesigner for allowing variable overrides.

The browser is broken into 5 'books' or sections which represent the 5 library types:

- *Unnamed Libraries:* Variables in unnamed libraries and/or open libraries that are not specified in any of your library paths
- *Local Libraries:* Timing libraries under the Local Paths and Libraries entry in the order they appear
- *Project Libraries:* Timing Libraries that are part of a currently open TimingDesigner project

- *Override Libraries:* Timing libraries specified under the Override Libraries entry in the order they appear

- *Root Path Libraries:* Timing libraries specified under the Library Root Paths entry in the order they appear

The books and libraries are displayed in hierarchical order from top to bottom representing how TimingDesigner searches for library values *[see chapter 25 of the TimingDesigner users guide for more details]*.

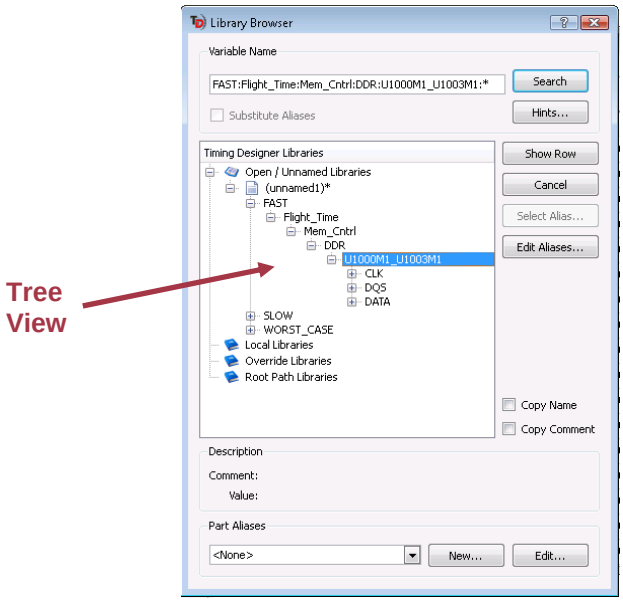


Figure 19: Library Browser with tree view

Variable Overrides

The new browser enables user a better view to understand how and where variables are being overridden. Since TimingDesigner users a hierarchical library search structure same named variables can occur in a search path with the variable higher in the hierarchy overriding the later.

This is useful so designers can override variables that they feel are incorrect for their particular project or diagram without having to change the original library and potentially cause issues for other users wanting to reference that library.

When a variable is being overridden TimingDesigner will now display in the browser an info icon so the user knows an override is occurring. The comment and value displayed in the description is referencing the higher level variable (or the value used if that variable is referenced in your diagram or project). If the user selects the info icon they will be presented with a dialog describing the override.

The override description displays the actual value of the variable you have selected as well as presents strategies to prevent this variable from being overridden if that is not desired.

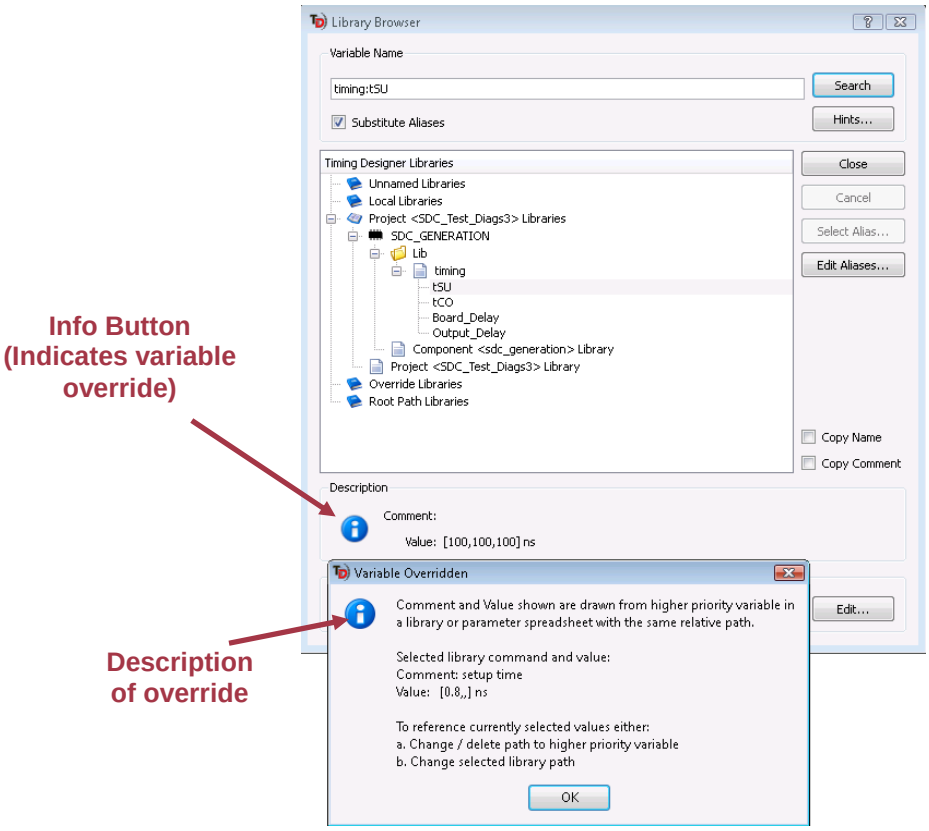


Figure 20: Library Browser Overrides

Library Window

Library Window has been updated to allow for a more Windows like operation.

The File pull down menu includes a new close all command which will close all open libraries at once. It has also been updated to display 'recently opened' libraries in the file pull down as opposed to referenced libraries to present a normal Windows operation.

Referenced libraries and open libraries are now presented in the library pull down menu.

Add Alias through Manager Window

Previously users were only able to add and modify Part Alias' through the library browser. Now users can also add, delete, and modify an Alias as well.

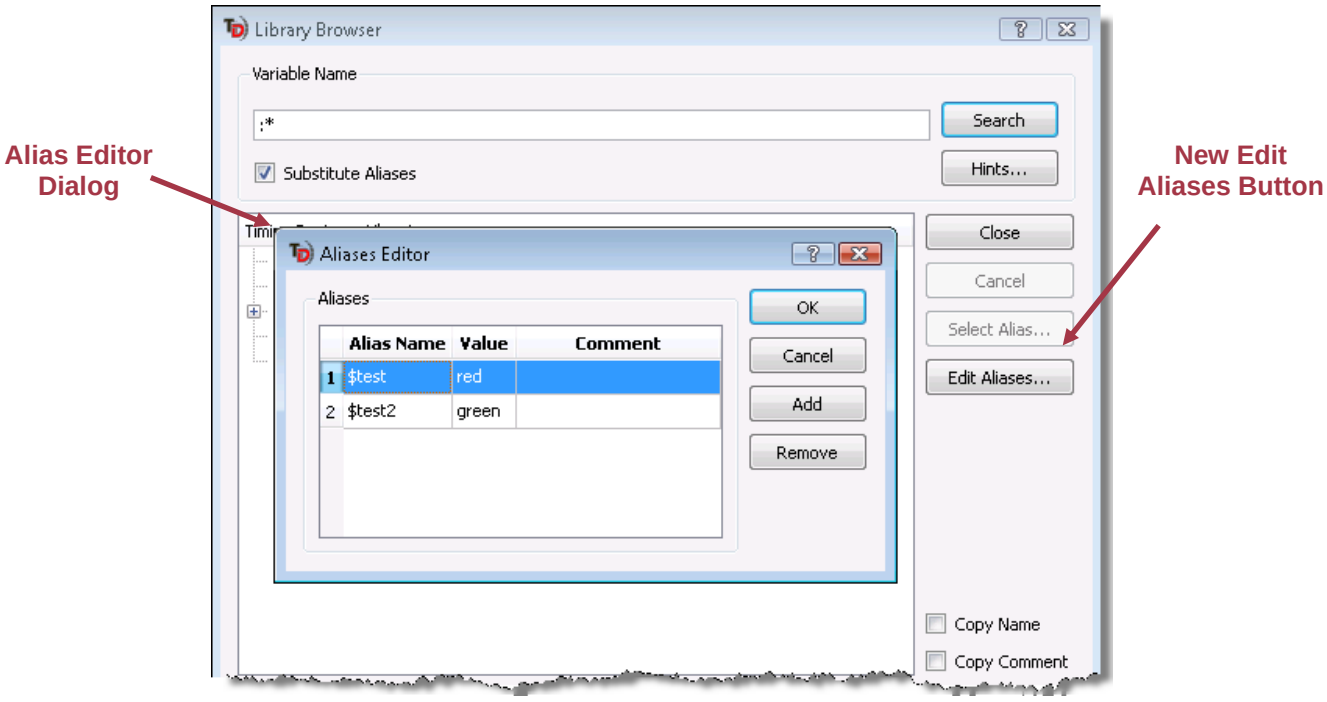


Figure 21: Adding Alias through library browser

The Alias editor will display all the Alias' currently in your diagram and will add an new alias; to your diagram that are created. Users can also swap values for their alias directly from the dialog.

New Icons

New Icons have been added to help users differentiate between file types and backup files

.TDP and .TDC icons

New project and component file icons

Backup file Icons

Grayscale icons have been added to differentiate backup files

Over 100 New Design Kits since Version 9.1 Released

EMA continues to support the design kit program and has made available over 200 new timing models since the initial release. These kits which provide a time saving head start in your interface timing design and analysis are available to all customers with a valid maintenance contract.

Users can log on to http://support.ema-eda.com to download available timing models

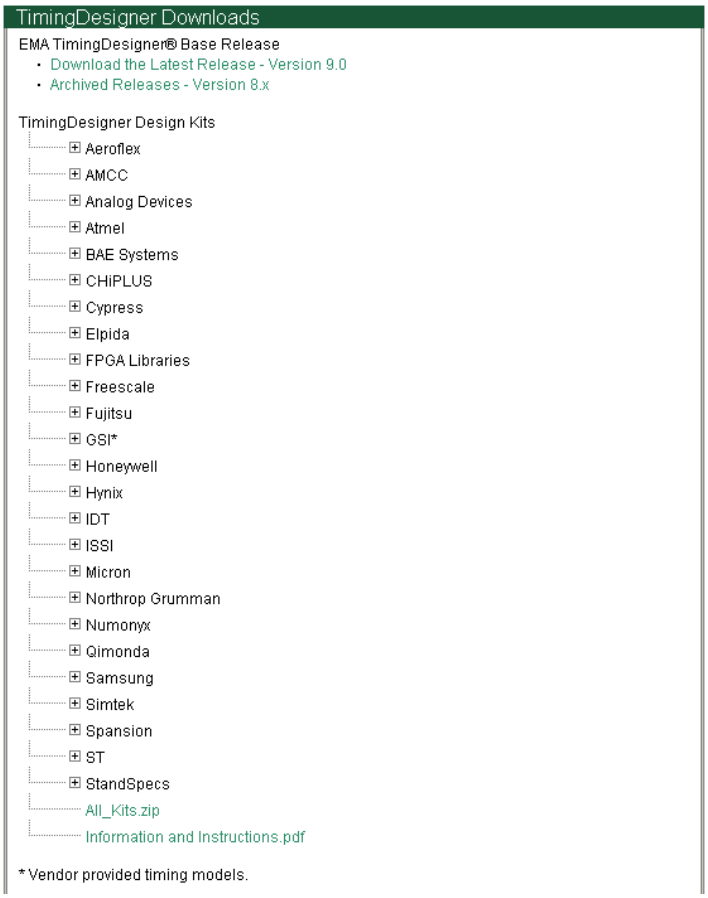


Figure 22 - Design Kit Page (EMA Support Site)

PCR's Fixed

12708 - EMF Export caused intermittent crash
12809 - TD not overwriting EMF file
12663 - OLE Export not scaling
12665 - Export to Clipboard Font Issue
12436 - Error when MIF export with Cause and Effect Marker
7571 - EPS export in Microsoft Word issues
12024 - MIF Export Issues
12025 - SVG Export Issues
12026 - EPS Export Issues
12581 - OLE Linking Issue
12629 - PDF export did not allow subset of signals to be exported
12807 - Error when superscript and subscript notation and exporting image
12808 - Winfont and Qfont not staying in synch
12690 - Printing diagram will cause printing loop
12723 - Alias change causes TimingDesigner to occasionally load all libraries
12488 - Library window freezes when dragged to the bottom of the page from parameter window
8852 - Lib Browser: Search to last selection variable on open.
12143 - Component library wont show contents until Project library has been selected
12589 - Restart required for new diagram to understand project library structure
9718 - Lib Win: TimingDesigner displaying all accessible libraries as opposed to all referenced and open libraries
9719 - Lib Win: Opened libraries that are referenced by the current diagram cannot be closed
12702 - Manager Win: Analysis Diagrams are renamed when opened from Manager window
12806 - Param Win: Rand() function not consistent across platforms
12712 - FPGA Tcl script generation not always recognizing valid signals and busses
12713 - Revision field added to Altera Tcl script generation
12826 - End Marker: When selecting to assign to new source, cursor becomes hour-glass
12710 - Adding new diagram dialog incorrect with more then one component in project
12054 - Context menu item to add new component.
12847 - Functions not resolving correctly when in a library path
12848 - Functions resolving value when it shouldn't

Where to Go for Help

Support

EMA Design Automation is committed to providing unsurpassed customer service and support. Our support site includes an extensive portfolio of TimingDesigner information to keep you productive. You'll get access to product downloads, a searchable knowledge base, online tutorials, training information, FAQs, user manuals and more. Please visit our website http://support.ema-eda.com to access more detailed information.

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