

ScanIO™-300LV Digital I/O Module

- Up to 300 (or 150 differential) boundary-scan controllable digital I/O lines per module (easily expandable with multiple modules)
- Each line is an independently controlled bi-directional signal and can be individually configured as an input or output
- JTAG ports and Digital I/O are configurable from 1.25V to 3.3V in 15 increments, and LVDS logic levels
- Each group of 50 I/O lines can be bypassed to save scan time for UUTs requiring less than 300 I/O lines
- Basic features are compatible with any IEEE 1149.1 compliant controller
- Supplied software contains BSDL files for integrating the ScanIO-300LV with the UUT
- Automatic test pattern generation is straightforward, no netlist modification or merging is required
- Compatible with existing automatic boundary-scan test pattern generators
- Applications include BSDL file verification and testing ICs, ASICs, MCMs, partially scan-testable boards, PCB edge connectors, non-scannable nets, clusters and cables



Figure 1. ScanIO-300LV Digital I/O Module

Introduction

The ScanIO-300LV digital I/O module turns an IEEE-1149.1 boundary-scan controller (such as the Corelis PCI-1149.1/Turbo™ or NetUSB-1149.1™) into a powerful digital interconnect and functional tester. It uses boundary-scan compatible ASICs to add control and visibility to connectors, traces, and logic that are otherwise untestable using traditional scan techniques. The ScanIO-300LV, combined with a boundary-scan controller, operates as a traditional "bed of nails" test system except access to the stimulus-and response I/Os is achieved via boundary-scan, and the size and the cost of the system are significantly smaller than traditional testers.

The ScanIO-300LV module provides a total of 300 fully bidirectional test channels with virtually unlimited memory depth per pin. Each line is independently controlled and can be

individually configured as an input or output. During testing, the programming and control of the test channels is automatically performed by the ScanPlus™/ScanExpress™ tools without any user intervention. The voltage level of the I/O and JTAG interfaces is programmable from 1.25V to 3.3V and supports either single ended or low voltage differential (LVDS) signaling.

Multiple ScanIO-300LV modules can be cascaded in series providing a sufficient number of pins for almost any digital test environment. By using single or multiple ScanIO-300LV modules, existing Automatic Test Pattern Generators (ATPGs) can be used to test non-scannable elements such as connectors, cables, and devices not incorporating boundary-scan. The ScanIO-300LV connects to the UUT inputs and outputs with standard flat-cables that can optionally be terminated with test probes.

Figure 2 shows a typical test configuration using the ScanIO-300LV module and a boundary-scan controller such as the Corelis PCI-1149.1/Turbo or NetUSB-1149.1. The scan chain originates from the scan controller, goes through the ScanIO-300LV, then through the UUT and back to the controller. Thus, a single scan chain can test not only all scannable elements on the UUT, but also the edge connector or other non-scannable elements.

Independent I/Os

All boundary-scan controlled digital I/O lines on the ScanIO-300LV are independently controllable and can be individually configured as inputs or outputs. Each module has a total of 300 I/O lines grouped in 6 blocks of 50 I/O lines each. Each block may be bypassed using the boundary-scan BYPASS command to reduce the scan time for UUTs that do not require the full 300 I/O lines. Multiple ScanIO-300LV modules can be linked together to provide the required number of signals for any sized test system.

The basic functionality of the ScanIO-300LV is fully compatible with the Corelis PCI-1149.1/Turbo, USB-1149.1/E™, NetUSB-1149.1, PCI-1149.1™ boundary-scan controller modules, as well as any IEEE Standard 1149.1 compliant boundary-scan controller module.

Adjustable Voltage Interface

The voltage level of the I/O and TAP interfaces is controlled by the adjustable rotary switch and can be set to any voltage between 1.25V and 3.3V in 15 increments.

The I/O voltage for each set of two connectors (J1/J2, J3/J4, J5/J6) may be individually configured from 1.25 to 3.3V in 0.05V increments when used with a PCI-1149.1/Turbo or NetUSB-1149.1 + ScanTAP-4™ controller.

The I/O and TAP interfaces are 3.3V tolerant at all voltage levels.

LVDS Voltage Interface

The I/O for each set of two connectors (J1/J2, J3/J4, J5/J6) can be configured as LVDS by setting the dip switch.

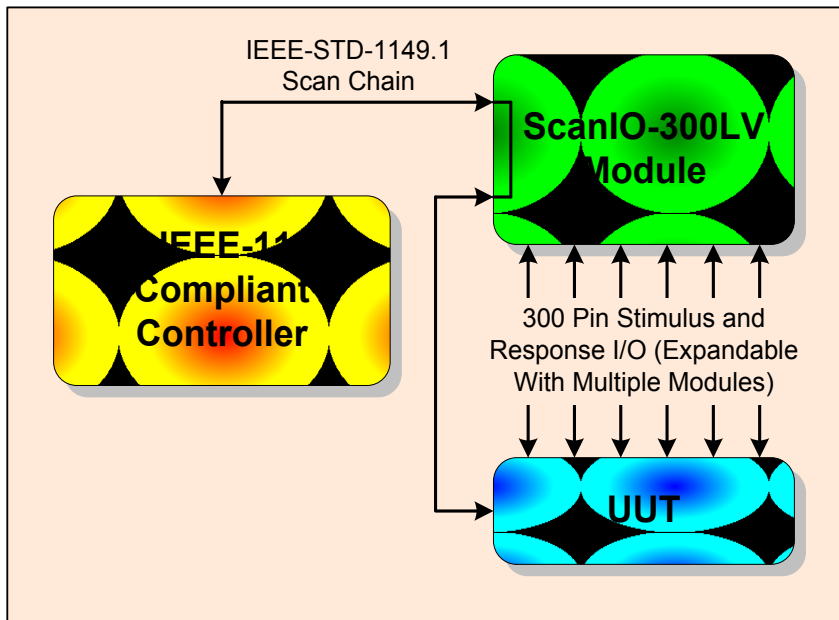


Figure 2. Single Chain Test Configuration

Testing Non-Scannable Elements

Use of the ScanIO-300LV allows a system designer to test, under boundary-scan control, certain non-scannable elements. Each bidirectional signal from or to the ScanIO-300LV can be used either to stimulate non-scannable test points such as edge connectors, cables, circuit board traces, pins on ASICs, or to respond to signals from those test points. In effect, the ScanIO-300LV generates virtual scan cells that can be used to replace or supplement pins in a "bed of nails" tester.

By properly laying out the desired board to be tested and "designing in" boundary-scan test points, it is possible to virtually eliminate the need for "bed of nails" testing. In those instances where a bed of nails tester is still necessary, the ScanIO-300LV can be used to augment the bed of nails tester by bringing a great deal of the discrete test points under boundary-scan control. This means that by using the ScanIO-300LV ASIC BSDL (Boundary-Scan Description Language) files, an Automatic Test Pattern Generator (ATPG) can generate test vectors to include non-scannable elements. The net result is that boards or modules can be much more thoroughly tested and elements such as edge connectors can now be included in the automatic test process.

Applications

The ScanIO-300LV can be included as an integral part of a complete test system. The ScanIO-300LV allows the benefits of automated boundary-scan testing to be extended to individual IC testing, board testing including edge connectors, cable testing, and in general areas of test that until now were not possible to test using boundary-scan.

A typical application can be an IC (ASIC, CPU, MCM, etc.) JTAG incoming inspection test system. In this instance, a ScanIO-300LV is used along with a 'Personality Module' containing a socket with a single boundary-scan compatible semiconductor device installed in it.

The test program is generated using the ScanIO-300LV BSDL file along with the BSDL file of the chip to be tested. The result is a test system that not only will test the internal boundary-scan path of the chip, but will also test the bonding of the semiconductor to the chip leads by exercising the electrical path between the outside leads of the chip and the internal semiconductor. A highly effective and efficient automated incoming inspection test system could thus be designed and put into place quite easily.

Test Pattern Generation

The BSDL files for the six ScanIO-300LV ASICs in the ScanIO-300LV are provided. Simply include the ScanIO-300LV BSDL files in the scan chain with the other boundary-scan components and use an automatic test pattern generator.

Self-Test

The ScanIO-300LV module is supplied with self-test vectors to verify proper operation of the module prior to testing the UUT. The self-test vectors are used with ScanPlus Runner to perform a ScanIO-300LV chain integrity test, test for shorts and opens, and can also perform an external loopback test. A set of 60-pin loopback cables is required to enable the loopback test. These cables connect sets of adjacent I/O connectors so a shorts/opens test can be performed.

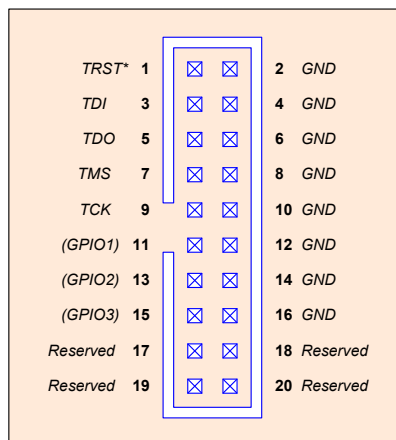


Figure 3. TAP Connector Pinout

Target TAP Connector

The TAP connector on the UUT should accommodate an industry standard 20-pin flat cable. Figure 3 shows the top view of the 20-pin target connector header (0.100" x 0.100" spacing). Standard 10-pin or 16-pin TAP connectors may also be used depending on the specific testing and in-system programming requirements. Please refer to Corelis application note 03-304 for additional details on these different connector formats. Corelis offers TAP interface cables to mate with many popular formats.

ScanIO-300LV Specifications:

TAP Interface

JTAG Compatibility	IEEE-1149.1
Maximum TCK Frequency	50 MHz
Programmable TAP Voltage	1.25V to 3.3V in 15 increments
Signal DC Characteristics	See Table 2

Boundary-scan Controlled I/O

Number of I/Os	300 digital I/O or 150 differential lines
Bypass Capability	Each block of 50 lines may be individually bypassed
Programmable I/O Voltage	1.25V to 3.3V in 15 increments ¹
Signal DC Characteristics	See Table 2

ScanIO Connectors

I/O Connectors (J1-J6)	20-pin shrouded header (0.1" x 0.1") (3M p/n 3428-6302 or equivalent)
I/O Connectors (J1-J6)	60-pin shrouded header (0.1" x 0.1") (3M p/n 3372-6302 or equivalent)

Mating Cable Connectors

I/O Connectors (J1-J6)	20-pin IDC socket with strain relief
I/O Connectors (J1-J6)	60-pin IDC socket with strain relief
Case Outline Dimensions	9.58 inches x 7.45 inches x 0.79 inches
Status Indicators	Voltage level LED display Configuration fault indicator

Power Requirements

From external supply (included)	5 Vdc @ 4 A (maximum)
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Operating Environment

Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non-condensing

Storage Environment

Temperature	-40°C to 85°C
Relative Humidity	0% to 95%, non-condensing

Note:

The I/O voltage for each set of two banks (J1/J2, J3/J4, J5/J6) may be individually configured from 1.25V to 3.3V in 0.05V increments when used with a PCI-1149.1/Turbo or NetUSB-1149.1 + ScanTAP-4 controller. Otherwise, the I/O voltage matches the TAP voltage.

Table 1. ScanIO-300LV General Specifications

Ordering information

The ScanIO-300LV Digital I/O module includes:

- ScanIO-300LV Module
- ScanIO-300LV User's Manual
- JTAG Controller TAP Interface Cable

- Target Interface Cables (x6)
- Power Supply
- Optionally, a CD-ROM containing the Corelis ScanExpress boundary-scan (JTAG) software

Symbol	Parameter	Test Conditions	Limit Min	Limit Max	Units
V_{CC} Adjust	Adjustable Voltage		1.3	3.4	V
V_{IH}	3.3V	V_{CC} Adjust \geq 2.5 V	2.0	3.6	V
	2.5V	$1.8 < V_{CC}$ Adjust $<$ 2.5 V	1.7	2.7	V
	1.8V	V_{CC} Adjust \leq 1.8 V	65% V_{CC} Adjust	1.95	V
V_{IL}	3.3V	V_{CC} Adjust \geq 2.5 V	-0.5	0.8	V
	2.5V	$1.8 < V_{CC}$ Adjust $<$ 2.5 V	-0.5	0.7	V
	1.8V	V_{CC} Adjust \leq 1.8 V	-0.5	35% V_{CC} Adjust	V
V_{IDIFF}	LVDS Differential Input Voltage	Common mode input voltage = 1.25 V	100	-	mV
V_{ICM}	LVDS Common-mode Input Voltage	Differential input voltage = \pm 350 mV	0.2	2.2	V
V_{OH}	3.3V	$I_{OH} = -24$ mA	2.4	-	V
	2.5V	$I_{OH} = -12$ mA	1.9	-	V
	1.8V	$I_{OH} = -8$ mA	V_{CC} Adjust - 0.4	-	V
	LVDS	100 Ω across P and N signals	1.25	1.6	V
V_{OL}	3.3V	$I_{OL} = 24$ mA	-	0.4	V
	2.5V	$I_{OL} = 12$ mA	-	0.4	V
	1.8V	$I_{OL} = 8$ mA	-	0.4	V
	LVDS	100 Ω across P and N signals	0.9	1.25	V
I_L	Input leakage current per pin	$V_I = V_{CC}$ or Ground	-10	10	μ A
I_{oz}	Tri-state output off-state current	$V_O = V_{CC}$ or Ground	-10	10	μ A

Table 2. ScanIO-300LV Electrical Specifications

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