CORELIS

USB-1149.1/4E™

High-Performance USB 2.0 Boundary-Scan and ISP Controller

- Supports I2C, JTAG, Microwire, SMbus and SPI interfaces
- High-speed USB 2.0 interface (up to 480 Mbits/sec signaling)
- High-performance In-System Programming (ISP) of Flash memories, Serial PROMs, CPLDs, FPGAs and other programmable devices
- High-performance boundary-scan controller
- User programmable JTAG TCK speeds up to 100 MHz
- Automatic signal delay compensation for long cable lengths to the UUT
- User programmable SPI/ Microwire SCK speeds up to 50 MHz
- User programmable I2C/ SMbus SCL speeds up to 5 MHz
- JTAG, SPI and I2C interfaces are individually programmable from 1.25 to 3.3V
- Easily connects to PCs and workstations via USB port
- Powered directly through the USB port; no need for an external power supply
- Built-in self-test features
- High-performance memory behind the pin architecture
- Firmware is field upgradeable
- Scan Function Library software for Windows 2000/XP
- Compatible with the optional ScanExpress™ family of products

Figure 1. USB-1149.1/4E Boundary-Scan and ISP Controller Hardware

Introduction

The Corelis USB-1149.1/4E™ is a sophisticated test controller that can be used in the testing of devices, boards, or systems, compliant with IEEE Standard 1149.1. Based on the Universal Serial Bus, the USB-1149.1/4E allows for the effortless connection of any JTAG-based target system to any PC or laptop hosting a USB port.

The Universal Serial Bus has gained wide spread popularity throughout the electronics community due to its incredible ease of connection. Devices like the USB-1149.1/4E, which are powered directly through the USB port, can be instantly connected to the host system by simply inserting a single USB cable.

Once connected, all features of the USB-1149.1/4E are completely accessible under software control. Three discrete I/O pins can be individually configured through software as standard inputs, outputs, or open collector drivers to test or control non-boundary-scan areas of the unit under test. Software controlled voltage translating logic allows the USB-1149.1/4E to be used to test low voltage systems.

A set of software drivers, written in C, is supplied with the USB-1149.1/4E device to allow the end users to create powerful test programs that are tailored to their specific needs.

Functional Description

The USB-1149.1/4E contains several performance enhancing functional sections aimed at increasing test vector throughput.

Key functional elements are the Enhanced Scan Engine with its flexible storage FIFOs and configurable Test Access Port (TAP) controller. This advanced architecture allows for the persistent feeding and extracting of scan vectors and completely decouples the clock-by-clock

scanning activity from the concurrent host USB download/upload operations. This proprietary architecture substantially increases scan vector throughput.

All functions of the USB-1149.1/4E are controlled by a state machine that contains status and control registers that can be accessed by user software through the USB port.

USB Interface

The Universal Serial Bus has gained wide spread popularity throughout the electronics community due to its incredible ease of connection and high-performance. The USB-1149.1/4E is a high-speed device compliant with Revision 2.0 of the USB Bus Specification (backward compatible with the full-speed features of Revision 1.1).

Devices like the USB-1149.1/4E, which are powered directly through the USB port, can be instantly connected to the host system by simply inserting a single USB cable.

Adjustable Low Voltage Outputs

The voltage level of the signal interface is software programmable and can be set to any voltage between 1.25V and 3.3V in increments of 0.05V. The voltage for each of the four TAPs may be set independently.

Variable Voltage Threshold

The input voltage threshold of the signals coming back from the target can be set for each TAP. The increased notice immunity allows the target to run more reliably at faster clock rates.

Scan Input Signal Delay Compensation

Automatic delay compensation is inserted within the signal paths for the JTAG and SPI interfaces. This feature is used to combat the well-know problems associated with the combination of high clock rates and remote target locations at extended distances.

Programmable Clocks

The clock rates for all programming interfaces are programmable under software control.

Target System Connection

The USB-1149.1/4E connection to the target is through four 20-pin connectors. The connectors are compatible with standard 20-pin IDC flat cable connectors. Test cables provided with the controller plug into the above header, ending in a 20-pin (0.050 × 0.100 in. spacing) target connector. This provides access to the JTAG, SPI and I2C signals.

Each interface can be arbitrarily assigned to a connector in software. Furthermore, the signals on the odd connector pins may be reassigned in software.

Power Requirements

The USB-1149.1/4E receives power from the host USB port according to that standard.

Pin	Signal Name			I/O	Description
1	TRST*	SDA	SCK	Input to UUT	JTAG Test Reset (optional), I2C Serial Data or SPI Serial Clock
3	TDI	SCL	MOSI	Input to UUT	JTAG Test Data Input, I2C Serial Clock or SPI Serial Data Input
5	TDO		MISO	Output of UUT	JTAG Test Data Output or SPI Serial Data Output
7	TMS		CS0*	Input to UUT	JTAG Test Mode Select or SPI Chip Select
9	TCK		CS1*	Input to UUT	JTAG Test Clock or SPI Chip Select
11	Write_Strobe*	GPIO1	CS2*	Input to UUT	Flash Programming Write Signal, General Purpose Output or SPI Chip Select
13	GPIO2	GPIO2	CS3*	Input to UUT	General Purpose Output or SPI Chip Select
15	Ready_Busy*	GPIO3	CS4*	Output of UUT	Flash Programming Ready Signal, General Purpose Output or SPI Chip Select
17	*reserved (do not connect)*				
18	*reserved (may be connected to GND)*				
19	*reserved (do not connect)*				
20	*reserved (may be connected to GND)*				

Notes: 1. Default pin assignments are shown; the odd pins are arbitrarily assignable in software.
2. Direction specified is relative to the UUT.
3. All other even pins of the connector (2, 4, 6, 8, 10, 12, 14 and 16) should be connected to ground (GND).

Table 1. USB-1149.1/4E 20-pin TAP Connector Pinout

Built-In Self-Test

The USB-1149.1/4E has built-in self-test capability. Logic has been provided at each I/O pin to loop back the signals from the target connector. This allows the electrical interface to be fully tested and enables comprehensive validation of its operation.

Scan Function "C" Library

Software drivers (Scan Function Library) and a self-test program are provided with the USB-1149.1/4E. The software is coded in 'C' and is provided as a 32-bit DLL for Windows 2000/XP. The software drivers provide the user with the functions that are necessary to operate the JTAG port and to send JTAG instructions and data to the target system. Users can incorporate the drivers in their own application software and only code the higher level test procedures.

The self-test software sends JTAG instruction and data words to the on-board boundary-scanned ICs. This code is the actual 'C' language code for the executable program TEST.EXE included on the disk.

The Scan Function Library (SFL) provided can be classified into two categories:

- Scanning
- Utility/Low-level access

The Scanning functions provide a higher level access to the operation of the USB-1149.1/4E. The table below lists all the SFL routines:

circulate_dr()

This function starts by flushing out data from a selected target's Data Register (DR) by scanning in the selected bit length + 16 zeros. Then the function will scan the flushed out data back into the target's Data Register DR.

get_driver_info ()

This function returns a string that indicates the version number of the scan function library and the revision of the firmware and hardware in the USB-1149.1/4E device.

hard_reset()

This function will perform a hard reset of all internal functions of the USB-1149.1/4E and transition the target TAPs into the Test-Logic-Reset state. This function should be called before all other scan function library function calls.

move_to_state()

Transitions the target JTAG device's state machine to the desired final stable state.

read_io()

This function reads the logical values that are sensed from the Discrete I/O pins.

scan_dr()

Scans data, from a specified array, out the USB-1149.1/4E and into the target JTAG device's Data Register (DR). Data that is scanned out of the target JTAG device's Data Register (DR) into the USB-1149.1/4E during the operation is stored in a specified array. The first bit scanned out is the LSB of the output array's first member. The first bit scanned in is stored in the LSB of the input array's first member. Following the scan operation, the device's JTAG state machine is left in the Run-Test/Idle state.

scan_ir()

Scans data, from a specified array, out the USB-1149.1/4E into the target JTAG device's Instruction Register (IR). Data that is scanned out of the target JTAG device's Instruction Register (IR) into the USB-1149.1/4E during the operation is stored in a specified array. The first bit scanned out is the LSB of the output array's first member. The first bit scanned in is stored in the LSB of the input array's first member. Following the scan operation, the device's JTAG state machine is left in the Run-Test/Idle state.

scan_Multiple ()

This is a "batch" function that will perform multiple commands of either Scan_IR, Scan_DR, Scan_to_Pause_IR, or Scan_to_Pause_DR. This function will execute substantially faster than issuing individual JTAG Scan commands, especially when a large number of small scans are involved.

scan_to_pause_dr()

Scans data, from a specified array, out the USB-1149.1/4E into the target JTAG device's Data Register (DR). Data that is scanned out of the target JTAG device's Data Register (DR) into the USB-1149.1/4E during the operation is stored in a specified array. The first bit scanned out is the LSB of the output array's first member. The first bit scanned in is stored in the LSB of the input array's first member. Following the scan operation, the device's JTAG state machine is left in the Pause-DR state.

scan_to_pause_ir()

Scans data, from a specified array, out the USB-1149.1/4E into the target JTAG device's Instruction Register (IR). Data that is scanned out of the target JTAG device's Instruction Register (IR) into the USB-1149.1/4E during the operation is stored in a specified array. The first bit scanned out is the LSB of the output array's first member. The first bit scanned in is stored in the LSB of the input array's first member. Following the scan operation, the device's JTAG state machine is left in the Pause-IR state.

set_scan_clk()

This function will set the TCK clock speed for JTAG operations. Note that the TCK is only present during tms_reset(), move_to_state() and scan operations.

set_tri_state()

This function sets the values applied to the selected tri-state pins to control the operation of the Discrete I/O and JTAG TAP pins.

set_trst()

This function sets the target's TRST* pin to the specified level.

set_voltage()

This function sets the output voltage for the discrete I/O and JTAG TAP pins.

test()

This function is a simple test of the application program's ability to execute library function calls. It simply returns the unsigned character passed into the function.

tms_reset()

Holds the TMS signal high for 5 TCKs to put the target's JTAG state machine into Test-Logic-Reset state.

USB-1149.1/4E Hardware Specifications:

Physical	
Mechanical Dimensions (enclosure)	3.8 ± 0.5 x 1.0 ± 0.5 x 4.6 ± 0.5 (inches)
Operating Environment	
Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non-condensing
Storage Environment	
Temperature	-40°C to 85°C
USB Interface	
USB Connector	Standard USB Type B Socket
Port Version	2.0
Power Requirements	
5.0V	Provided by the host USB 2.0 port
LEDs	
Blue LED	Indicates the USB-1149.1/4E is powered and initialized
Target Interface	
Connectors	AMP P/N 5-104069-1 (0.050 x 0.100 inches)
Programmable Output Voltage	1.25 to 3.3V, in 0.5V steps
Programmable Threshold Voltage	1.25 to 3.3V, in 0.5V steps
JTAG Interface	
Compliance	IEEE-1149.1 compliant interface
Maximum TCK Clock Frequency	100 MHz
I2C Interface	
Maximum SCL Clock Frequency	5 MHz
SPI Interface	
Supported Chip Selects	Up to 8
Maximum SCK Clock Frequency	50 MHz
Target Assisted Flash Programmer Interface	
Supported CPUs	Please contact Corelis for currently supported CPUs

Table 2. USB-1149.1/4E Hardware Specifications

Adjustable Voltage	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
3.3	-0.3	0.8	2.0	3.6	0.4	2.9	16	-16
2.5	-0.3	0.7	1.7	3.6	0.4	2.1	16	-16
1.8	-0.3	0.6	1.2	3.6	0.4	1.4	16	-16
1.5	-0.3	0.5	1.0	3.6	0.4	1.1	8	-8
1.2	-0.3	0.4	0.8	3.6	0.4	0.8	6	-6

Table 3. USB-1149.1/4E Signal DC Characteristics

Ordering Information

The USB-1149.1/4E (P/N 10390) includes the following:

- USB-1149.1/4E hardware
- One 10-pin standard target interface cable (12")
- One 6 foot USB cable (2.0 standard)
- A CD-ROM containing support software and example target test files
- USB-1149.1/4E User's Manual
- Optionally, a CD-ROM containing the ScanExpress boundary-scan (JTAG) and in-system programming software tools

The following optional cables are also available separately:

- 10-pin standard target interface cable (12") [P/N: 15390-2]
- 16-pin standard target interface cable (12") [P/N: 15391-2]
- 20-pin standard target interface cable (12") [P/N: 15392-2]
- 16-pin PowerPC target interface cable (12") [P/N: 15393-2]
- 20-pin ARM target interface cable (12") [P/N: 15394-2]

ScanExpress Family

Corelis has a complete family of boundary-scan test and in-system-programming tools. Corelis' complete family of ScanExpress tools provides a user with the ability to perform comprehensive boundary-scan interconnect testing and in-system-programming of CPLDs, FPGAs, and Flash memory devices.

Software is available for infrastructure and interconnects testing of both boards and systems. Boundary-scan defect testing is particularly useful for finding stuck-at faults, opens, shorts, and bridging faults when using BGA components or other fine pitch, difficult to probe, packages.

The ScanExpress family of tools includes an automatic boundary-scan Scan Test Pattern Generator (ScanExpressTPG), boundary-scan test execution and in-system-programming software (ScanExpress Runner), and a boundary-scan interactive debugger (ScanExpress Debugger).

The ScanExpressTPG automatically generates test patterns that enable testing of boundary-scan chain integrity, PCB interconnects, buswires, and clusters including memories and FIFOs. These test vectors are then applied to the Unit Under Test through one of the Corelis boundary-scan controllers.

The ScanExpress comprehensive diagnostics package provides the location of the fault in the user's terms for netlist, IC name, and pin number.

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