

NetUSB-1149.1/SE™ High-Performance LAN/USB 2.0 Boundary-Scan Controller

- Concurrent (gang) testing and in-system programming of CPLDs and Flash devices on up to 8 boards
- User programmable sustained Test Clock (TCK) up to 80 MHz, in <2% increment per TAP, at an effective throughput of 640 MHz
- Hardware comparison of expected patterns against observed results is done concurrently for each TAP
- Easily connects to PCs and workstations via USB port or 10/100Base-T Ethernet
- High-speed device (up to 480 Mbps signaling) compliant with Revision 2.0 of the USB Specification
- Pre-power up test for shorts between power and ground lines on the UUT for each TAP
- Analog voltage measurement of +/- 50V
- TAP signals and GPIO discrete signals are individually programmable from 1.3V to 3.3V (5 volt tolerant)
- Variable threshold on TDO coming back from the UUT for increased noise margin
- Direct Write signal for expediting Flash programming
- Support for monitoring Flash RDY/BSY
- USB and Ethernet connection allow extended distance from PC to UUT- no TAP extenders are needed
- Automatic signal delay compensation for long cable lengths to the UUT
- Plug and Play Windows 2000/XP device drivers
- Fully compatible with the ScanPlus and ScanExpress families of products



Figure 1. NetUSB-1149.1/E Boundary-Scan Controller

Introduction

In the last few years, the use of boundary-scan has expanded beyond traditional board test applications into in-system programming of CPLDs, FPGAs, and Flash memories. These new applications require much higher performance.

Until now, available products were limited in Test Clock (TCK) frequency and the comparison of the expected patterns with the observed results was done by the host computer. Now that boards include more and denser memories including flash, users are asking for higher throughput boundary-scan tools that will allow faster testing and in-system programming. This includes concurrent (often referred to as gang) testing and in-system programming of more than one board at a time.

In response to this need, major development efforts in Boundary-Scan technology were undertaken at Corelis. The success of this development has produced a quantum

leap in scan vector throughput, maintaining Corelis as the clear leader in providing sophisticated yet easy to use Boundary-Scan test equipment.

A key element of this ground breaking technology is the NetUSB-1149.1/SE™ controller which dramatically increases the test and in-system programming speed by applying a vast number of innovative and proprietary techniques developed at Corelis.

The result of these new techniques allows for an unsurpassed boundary-scan throughput at TCK frequencies reaching a sustained 80MHz rate and a scan efficiency of 100% at each of up to eight concurrently scanning JTAG ports.

Corelis thus presents the NetUSB-1149.1/SE High-Performance Boundary-Scan Test and In-System Programming Controller, as the premier solution for users whose applications demand the highest possible scan vector throughput that is currently available on the market.

General Description

The NetUSB-1149.1/SE is an advanced robust controller that can be used in the testing and/or in-system programming (ISP) of devices, boards, or systems compliant with the IEEE-1149.1 standard. The controller connects to the computer either through its USB interface or LAN interface for easy installation at close or remote locations.

The NetUSB-1149.1/SE controller contains several performance enhancing functional sections aimed at increasing test vector and in-system programming throughput. The combination of these functional elements results in a very high data-scanning rate, which is completely decoupled from the USB and Ethernet interfaces. The scanned patterns are distributed to the target device or devices via the TAP interfaces on the controller.

The NetUSB-1149.1/SE controller can apply test vectors and/or ISP patterns to boards with a variety of JTAG chain topologies. In the simplest, yet often used case, the controller will provide the interface between the computer and a target system consisting of a single JTAG Test Access Port (TAP). This would be the case where the target system consists of one JTAG chain and its associated TAP.

If the board under test consists of groups that include multiple devices, each with their own respective TAP, then the NetUSB-1149.1/SE allows for test vectors to be applied to each of the target TAPs individually, one TAP at a time, or jointly to all of the TAPs. Figure 1 depicts such a configuration.

Figure 2 depicts a case where the NetUSB-1149.1/SE is connected to eight identical boards. In this case the system can test and program the eight boards concurrently. Note that the concept of concurrency here not only applies to the simultaneous application of test vectors and ISP patterns to each board but also applies to the simultaneous verification of each individual board. A failure on any of the individual boards will be properly logged and will not prohibit the continuation of testing on the remaining target devices. The concurrent (often referred to as gang) mode of operation offers great performance in-

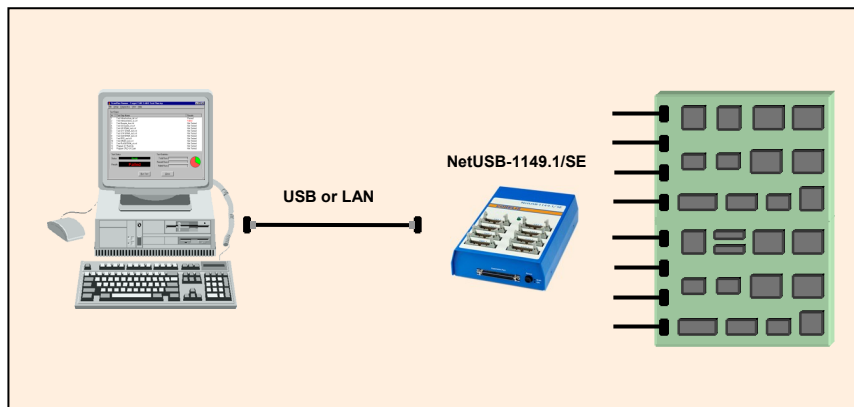


Figure 1. Connection to a single UUT with eight TAPs

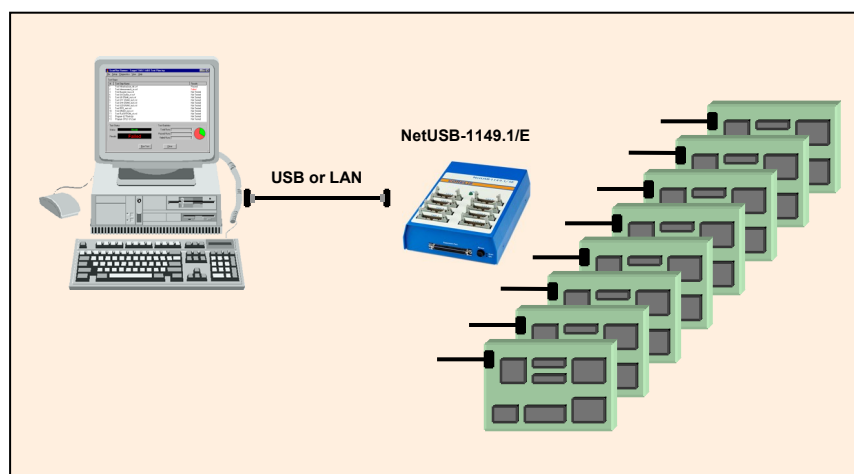


Figure 2. Connection to eight UUTs with a single TAP each

creases when testing, in-system programming, and verifying multiple targets.

Programmable Clock

The system-wide TCK rate for all TAP ports is programmable under software control. A wide range of TCK frequencies can be achieved by using the on-board Phase-Locked-Loop (PLL) generation circuitry. The user is given the ability to select the desired TCK rate from a range of values from 50 KHz to 80 MHz at resolution increments of less than 2%.

Adjustable Low Voltage Outputs

The voltage level of each TAP is software programmable and can be set to any voltage between 1.3V and 3.3V in increments of 0.05V. The ports of the NetUSB-1149.1/SE

can also be slew rate (fast/slow) adjusted.

Variable Voltage Threshold

The input voltage threshold of TDO coming back from the target can be set for each TAP. The increased noise immunity allows the target to run reliably at faster TCK rates.

Scan Input Signal Delay Compensation

Automatic delay compensation is inserted within the signal paths. This feature is used to combat the well-known problems associated with the combination of high TCK rates and remote target locations at extended distances.

Target Voltage Detection System

The NetUSB-1149.1/SE includes

analog-to-digital converters, which can measure connected power voltages of up to +/- 50V from the target. Such voltages can be measured and compared against user-defined limits. This feature can provide detailed signal voltage checks at any stage of a test plan.

Automatic Detection of Target Power Shorts

With the target powered down, a well-regulated drive current with current limit can be momentarily applied to the target power bus. By measuring this current, the approximate load resistance can be calculated. This provides for the automatic detection of target power shorts, prior to applying power to the target unit.

Parallel Input/Output Ports

Each TAP connector contains 3 general purpose parallel I/O signals (GPIOs) whose direction and drive (totem-pole or open-collector) is configurable. The input and output ports can be used to control and sense various functions in the target system which cannot be controlled or observed through boundary-scan operations. These ports are useful for the testing of target systems that incorporate components that are not compliant to IEEE Standard 1149.1. Open-collector signals are often needed to drive reset and emulation signals.

Built-in Self-Test

The NetUSB-1149.1/SE has a built-in self-test capability. Logic has been provided at the local TAP connector to loop back data shifted out on TMS and TDO.

USB Interface

The NetUSB-1149.1/SE can connect to the host PC computer via its USB interface. The NetUSB-1149.1/SE is a high-speed device compliant with Revision 2.0 of the USB Bus Specification (backward compatible with the full-speed features of Revision 1.1).

Ethernet Interface

The NetUSB-1149.1/SE can also connect to the host PC computer or workstation via a standard

Pin	Signal Name	I/O	Description
1	TRST*	Out	Test Reset Output to UUT
3	TDI	Out	Test Data Output to UUT
5	TDO	In	Test Data Input from UUT
7	TMS	Out	Test Mode Select Output to UUT
9	TCK	Out	Test Clock Output to UUT
11	Write_Strobe* (GPIO1)	I/O	Write Strobe Output to UUT. Discrete I/O to/from UUT
13	GPIO2	I/O	Discrete I/O to/from UUT
15	Ready/Busy* (GPIO3)	I/O	Flash Ready/Busy* polling. Discrete I/O to/from UUT
17	VCC1	In	UUT Power Test Point 1
19	reserved	-	

Table 1– NetUSB-1149.1/SE 20-pin Connector

Note: Direction specified is relative to pod. All other pins of the connector (2,4,6,8,10,12,14,16,18,and 20) are connected to ground (GND).

10/100BaseT LAN interface. The Ethernet interface is IEEE 802.3u 100BASE-FX compatible with automatic speed switching, accessed through an RJ-45 connector.

plied by Corelis such as the ScanTAP-32™. Using this expansion port, the number of TAPs supported by the controller can be expanded.

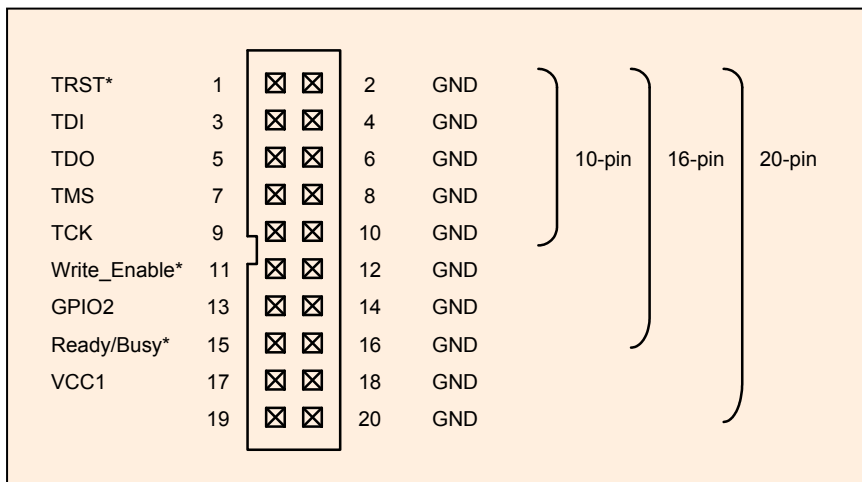
Compatible with ScanPlus Family of Products

The NetUSB-1149.1/SE is both hardware and software compatible with the complete ScanPlus™ and ScanExpress™ family of IEEE-1149.1 test and in-system programming products.

TAP Connectors

The NetUSB-1149.1/SE contains eight 20-pin TAP connectors. All eight connectors have the same signals and the same pinout. Each connector is a shrouded header (0.100 × 0.100 in. spacing) with long ejectors that are compatible with standard 20-pin IDC flat cable connectors (with strain relief). Note that only the first 10 pins are required for basic boundary-scan operation. For Flash Programming with external

The NetUSB-1149.1/SE also contains an expansion port that is compatible with other equipment sup-



NetUSB-1149.1/E target connector pin assignments for various TAP cables

write or the Ready Busy signal, use the first 16 pins of the TAP. To build in support for power-to-ground short checking, use all 20 pins of the TAP.

Pins 17 each NetUSB-1149.1/SE TAP connector can be used to sense that the target power pin is not shorted to GND. Different power pins can be checked on each of the eight 20-pin connectors of the NetUSB-1149.1/SE controller.

The 3 GPIO signals are general-purpose output signals that are directly controlled by the Parallel I/O menu of ScanPlus Runner. The dual purpose Write_Strobe* (GPIO1) signal is used for Flash programming, and if used will override the Parallel Output (GPIO1) function. The dual purpose Ready/Busy* (GPIO3) signal is used for Flash programming, and if used will override the Parallel Output (GPIO3) function.

For the target design, it is recommended that an industry-standard 10-pin, 16-pin or 20-pin TAP connector format be used, depending on the specific testing and in-system programming requirements. Refer to Corelis application note 03-304 for additional details on these different connector formats. Corelis offers TAP cables to mate with all of these different formats.

Ordering information

NetUSB-1149.1/SE (P/N 10339) includes:

- NetUSB-1149.1/SE Hardware Controller
- NetUSB-1149.1/SE User's Manual
- NetUSB-1149.1/SE Software Disk
- Eight 20-pin to 10-pin target cables
- Power Supply

NetUSB-1149.1/SE Specifications:

Host Computer Requirements

CPU	Pentium III @ 1GHz or better
Operating System	Windows 2000 SP4 or Windows XP

USB Interface

Version	Revision 2.0 high-speed device (backward compatible with the full-speed features of Revision 1.1)
---------	---

Ethernet Interface

Version	IEEE 802.3u 100BASE-FX
---------	------------------------

TAP Interface

Version	IEEE-1149.1
Connectors	Eight 20-pin shrouded headers, 0.1 in. x 0.1 in. spacing (3M 3428-6302 or equivalent)
Number of TAPs	8
Maximum TCK frequency	80 MHz
Maximum scanning data length	Unlimited
TCK frequency steps	1.00 MHz increments between 25 and 80 MHz, 0.50 MHz increments between 12.5 and 25 MHz, 0.25 MHz increments (or less) below 12.5 MHz
Programmable Interface Voltage	1.25 to 3.3 V in 0.05 V increments
Programmable TAPs	Each set of 2 TAPs (1/4, 2/5, 3/6, 4/8) has its own programmable volt-

Signal DC characteristics	See Table 2
---------------------------	-------------

Physical

Case Outline Dimensions	5.2 in. x 7.1 in. x 1.9 in.
-------------------------	-----------------------------

Power Short Test Pins

Power (Vcc) Sense Pins	One per TAP (Vcc1), 8 total
Vcc Measurement Type	Short to GND detect; Voltage sensing, Target unpowered
Voltage Sense Resolution	12-bit ADC
Voltage Sense Accuracy	+/- 50 mV

I/O Connectors

USB Connector	Standard USB type B socket
Ethernet Connector	Standard RJ-45 socket
Expansion Connector	68-pin SCSI II type (AMP P/N 787171-7 or equivalent)

Power Requirements

From external supply (included)	5 Vdc @ 4 A maximum
---------------------------------	---------------------

Operating Environment

Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non-condensing

Storage Environment

Temperature	-40°C to 85°C
Relative Humidity	0% to 95%, non-condensing

Symbol	Test Conditions	Limit Min	Limit Max	Units
V _{IH}	V _{DD} Adjust >= 2.5 V	2	V _{DD} + 0.5	V
	V _{DD} Adjust < 2.5 V	0.65 × V _{DD}	V _{DD} + 0.5	V
V _{IL}	V _{DD} Adjust >= 2.0		0.7	V
	V _{DD} Adjust <= 2.0		0.35 × V _{DD}	V
V _{OH}	I _{OH} = -2 mA	V _{DD} - 0.35		V
V _{OL}	I _{OL} = 2 mA V _{DD} = 1.65 V		0.45	V
I _{OH}	V _{DD} = 1.65 - 1.95 V		-4	mA
I _{OL}	V _{DD} = 1.65 - 1.95 V		4	mA

Table 2– NetUSB-1149.1/SE TAP DC Characteristics

CORELIS

13100 Alondra Blvd.
Cerritos, California 90703
 Telephone: (562) 926-6727, Fax: (562) 404-6196
sales@corelis.com www.corelis.com