CORELIS

USB-1149.1/E™

USB 2.0 Boundary-Scan Controller

- High-performance plug-and-play IEEE-1149.1 Boundary-Scan (JTAG) controller for the Universal Serial Bus (USB 2.0)
- High-speed (up to 480 Mbit/sec signaling) device compliant with Revision 2.0 of the USB Specification (backward compatible with the Full-speed features of USB Revision 1.1)
- Easily connects to PCs and workstations via USB port
- Powered directly through the USB port; no need for external power supply
- High-performance memory behind the pin architecture
- JTAG port and parallel I/O are programmable from 1.25 to 3.3V and are 5V compatible
- User programmable test clock (TCK) with speeds up to 100 MHz
- 3 general purpose programmable parallel I/O lines for remote UUT control and sense
- Direct Write signal for expediting Flash programming
- Support for monitoring Flash RDY/BSY
- Automatic signal delay compensation for long cable lengths to the UUT
- Scan Function Library software for Windows 2000/XP
- Plug and play Windows 2000/XP device drivers
- Built-in self-test features
- Compatible with the optional ScanExpress™ family of products for testing and in-system programming of Flash memories and CPLDs

Figure 1. USB-1149.1/E Boundary-Scan Controller

Introduction

The Corelis USB-1149.1/E™ is a sophisticated test controller that can be used in the testing of devices, boards, or systems, compliant with IEEE Standard 1149.1. Based on the Universal Serial Bus, the USB-1149.1/E allows for the effortless connection of any JTAG-based target system to any PC or laptop hosting a USB port.

The Universal Serial Bus has gained wide spread popularity throughout the electronics community due to its incredible ease of connection. Devices like the USB-1149.1/E, which are powered directly through the USB port, can be instantly connected to the host system by simply hand-inserting a single USB cable.

Once connected, all features of the USB-1149.1/E are completely accessible under software control. Three discrete I/O pins can be individually configured through software as standard inputs, outputs, or open collector drivers to test or control non-boundary-scan areas of the unit under test. Software controlled voltage translating logic allows the USB-1149.1/E to be used to test low voltage systems.

A set of software drivers, written in C, is supplied with the USB-1149.1/E device to allow the end users to create powerful test programs that are tailored to their specific needs.

Functional Description

The USB-1149.1/E contains several performance enhancing functional sections aimed at increasing test vector throughput.

Key functional elements are the Enhanced Scan Engine with its flexible storage FIFOs and configurable Test Access Port (TAP) controller. This advanced architecture allows for the persistent feeding and

extracting of scan vectors and completely decouples the clock-by-clock scanning activity from the concurrent host USB download/upload operations. This proprietary architecture substantially increases scan vector throughput.

All functions of the USB-1149.1/E are controlled by a state machine that contains status and control registers that can be accessed by user software through the USB port.

Programmable Clocks

The USB-1149.1/E TCK output to the IEEE Standard 1149.1 compatible target system is programmable under software control. A wide range of TCK frequencies from 1 to 100 MHz can be achieved by using the on-board TCK generation circuitry. Delay compensation for the returning TDI bit stream can be added under software control to greatly increase the workable TCK frequency.

Adjustable Low Voltage Outputs

The voltage level of the parallel I/O and the TAP interface is software programmable and can be set to any voltage between 1.25V and 3.3V in increments of 0.05V. These interfaces are 5V compatible and 5V tolerant at all programmed levels.

Parallel Input/Output Ports

Three discrete I/O pins can be individually configured through software as standard inputs, outputs, or open collector drivers to test or control non-boundary-scan areas of the unit under test. This is accomplished by providing direct software control to drive, sense, and tri-state each of the three pins.

The input and output pins can be used to control and sense various functions in the target system which cannot be controlled or observed through boundary-scan operations. These pins are useful for testing of target systems that incorporate components that are not compliant to IEEE Standard 1149.1.

Built-in Self-Test

The USB-1149.1/E has a built-in self-test capability. Logic has been provided at the JTAG connector to read back, synchronously with TCK, data shifted out on TMS and TDO on the JTAG TAP. Similarly, loop-back logic has been provided to drive and sense each of the discrete I/O pins. In this way the complete electrical interface at the JTAG TAP can be fully tested.

USB Interface

The USB-1149.1/E is a high-speed device compliant with Revision 2.0 of the USB Bus Specification (backward compatible with the full-speed features of Revision 1.1).

Scan Function "C" Library

Software drivers (Scan Function Library) and a self-test program are provided with the USB-1149.1/E. The software is coded in ‘C’ and is provided as a 32-bit DLL for Windows 2000/XP. The software drivers provide the user with the functions that are necessary to operate the JTAG port and to send JTAG instructions and data to the target system. Users can incorporate the drivers in their own application software and only code the higher level test procedures.

The self-test software sends JTAG instruction and data words to the on-board Boundary-scanned ICs. This code is the actual ‘C’ language code for the executable program TEST.EXE included on the disk.

The Scan Function Library (SFL) provided can be classified into two categories:

- Scanning
- Utility/Low-level access

The Scanning functions provide a higher level access to the operation of the USB-1149.1/E. The table below lists all the SFL routines:

circulate_dr()

This function starts by flushing out data from a selected target’s Data Register (DR) by scanning in the selected bit length + 16 zeros. Then the function will scan the flushed out data back into the target’s Data Register DR.

get_driver_info ()

This function returns a string that indicates the version number of the scan function library and the revision of the firmware and hardware in the USB-1149.1/E device.

hard_reset()

This function will perform a hard reset of all internal functions of the USB-1149.1/E and transition the target TAPs into the Test-Logic-Reset state. This function should be called before all other scan function library function calls.

move_to_state()

Transitions the target JTAG device’s state machine to the desired final stable state.

read_io()

This function reads the logical values that are sensed from the Discrete I/O pins.

scan_dr()

Scans data, from a specified array, out the USB-1149.1/E and into the target JTAG device’s Data Register (DR). Data that is scanned out of the target JTAG device’s Data Register (DR) into the USB-1149.1/E during the operation is stored in a specified array. The first bit scanned out is the LSB of the output array’s first member. The first bit scanned in is stored in the LSB of the input array’s first member. Following the scan operation, the device’s JTAG state machine is left in the Run-Test/Idle state.

scan_ir()

Scans data, from a specified array, out the USB-1149.1/E into the target JTAG device’s Instruction Register (IR). Data that is scanned out of the target JTAG device’s Instruction Register (IR) into the USB-1149.1/E during the operation is stored in a specified array. The first bit scanned out is the LSB of the output array’s first member. The first bit scanned in is stored in the LSB of the input array’s first member. Following the scan operation, the device’s JTAG state machine is left in the Run-Test/Idle state.

scan_Multiple ()

This is a “batch” function that will perform multiple commands of either Scan_IR, Scan_DR, Scan_to_Pause_IR, or Scan_to_Pause_DR. This function will execute substantially faster than issuing individual JTAG Scan com-

mands, especially when a large number of small scans are involved.

scan_to_pause_dr()

Scans data, from a specified array, out the USB-1149.1/E into the target JTAG device's Data Register (DR). Data that is scanned out of the target JTAG device's Data Register (DR) into the USB-1149.1/E during the operation is stored in a specified array. The first bit scanned out is the LSB of the output array's first member. The first bit scanned in is stored in the LSB of the input array's first member. Following the scan operation, the device's JTAG state machine is left in the Pause-DR state.

scan_to_pause_ir()

Scans data, from a specified array, out the USB-1149.1/E into the target JTAG device's Instruction Register (IR). Data that is scanned out of the target JTAG device's Instruction Register (IR) into the USB-1149.1/E during the operation is stored in a specified array. The first bit scanned out is the LSB of the output array's first member. The first bit scanned in is stored in the LSB of the input array's first member. Following the scan operation, the device's JTAG state machine is left in the Pause-IR state.

set_io()

This function sets the output levels of the selected Discrete I/O pins.

set_scan_clk()

This function will set the TCK clock speed for JTAG operations. Note that the TCK is only present during tms_reset(), move_to_state() and scan operations.

set_tri_state()

This function sets the values applied to the selected tri-state pins to control the operation of the Discrete I/O and JTAG TAP pins.

set_trst ()

This function sets the target's TRST* pin to the specified level.

set_voltage ()

This function sets the output voltage for the Discrete I/O and JTAG TAP pins.

test()

This function is a simple test of the application program's ability to execute library function calls. It simply returns the unsigned character passed into the function.

Pin	Signal Name	I/O	Description
1	TRST*	Out	Test Reset Output to UUT
3	TDI	Out	Test Data Input to UUT
5	TDO	In	Test Data Output from UUT
7	TMS	Out	Test Mode Select Output to UUT
9	TCK	Out	Test Clock Output to UUT
11	Write_Strobe* (GPIO1)	I/O	Write Strobe Output to UUT. Discrete I/O to/from UUT
13	GPIO2	I/O	Discrete I/O to/from UUT
15	Ready/Busy* (GPIO3)	I/O	Flash Ready/Busy* polling. Discrete I/O to/from UUT
17	Reserved		Reserved
19	Reserved		Reserved

Figure 2. USB-1149.1/E 20-pin Connector

Note: Direction specified is relative to pod. All other pins of the connector (2,4,6,8,10,12,14,16,18,and 20) are connected to ground (GND).

Parameter	Conditions	MIN	MAX	UNIT
High Level Input Voltage (V_{IH})	V_{CC} = 1.25V	1.25	5.5	V
	V_{CC} > 2.7V	2		V
Low Level Input Voltage (V_{IL})	V_{CC} = 1.25V	0	0	V
	V_{CC} > 2.7V		0.8	V
Output High Level Voltage (V_{OH})	I_{OH} = -12mA	Vcc-0.5		V
	I_{OH} = -0.1mA	Vcc-0.2		V
Output Low Level Voltage (V_{OL})	I_{OL} = 12mA		0.4	V
	I_{OL} = 0.1mA		0.2	V
Input Leakage Current (I_I)	$V_I = V_{cc}$		0.1	µA
	V_I = GND	-700		µA

Figure 3. I/O and TAP Signal Characteristics

tms_reset()

Holds the TMS signal high for 5 TCKs to put the target's JTAG state machine into Test-Logic-Reset state.

Compatible with ScanExpress Family of Products

The USB-1149.1/E is both hardware and software compatible with the complete ScanExpress™ family of IEEE-1149.1 test and in-system programming products (see Figures 4 and 5). Consequently, test programs developed for other Corelis tester platforms will run on the USB-1149.1/E and vice-versa.

Specifications

Size
3.0" x 2.0" x 0.5"

Logic Levels
Outputs CMOS (programmable 1.25

to 3.3V). Inputs TTL

Max TCK clock frequency
100 MHz

I/O Connectors
JTAG Connector (TAP) 20-pin IDC (3M part no. 3428-5602 or equiv.)

JTAG Interface
IEEE-1149.1 compliant interface

Power
Supplied by USB host

Operating environment
Temperature 0 to 55C. Relative humidity 10% to 90%, non condensing

Storage environment
Temperature -40 to +85C

Ordering Information

USB-1149.1/E (P/N 10342R) that includes:

- USB-1149.1/E Hardware
- USB-1149.1/E User's Manual
- USB-1149.1/E Software Disk
- One 20-pin to 10-pin target cable
- One 20-pin to 16-pin target cable
- One 20-pin to 20-pin target cable

ScanExpress Family

Corelis has a complete family of boundary-scan test and in-system-programming tools. The complete Corelis' family of ScanExpress tools provides a user with the ability to perform comprehensive boundary-scan interconnect testing and in-system-programming of CPLDs, FPGAs, and Flash memory devices. Software is available for infrastructure and interconnects testing of both boards and systems. Boundary-scan defect testing is particularly useful for finding stuck-at faults, opens, shorts, and bridging faults when using BGA components or other fine pitch, difficult to probe, packages.

The ScanExpress family of tools includes an automatic boundary-scan Test Pattern Generator (ScanExpressTPG), boundary-scan test execution and in-system-programming software (ScanExpress Runner), and a boundary-scan interactive debugger.

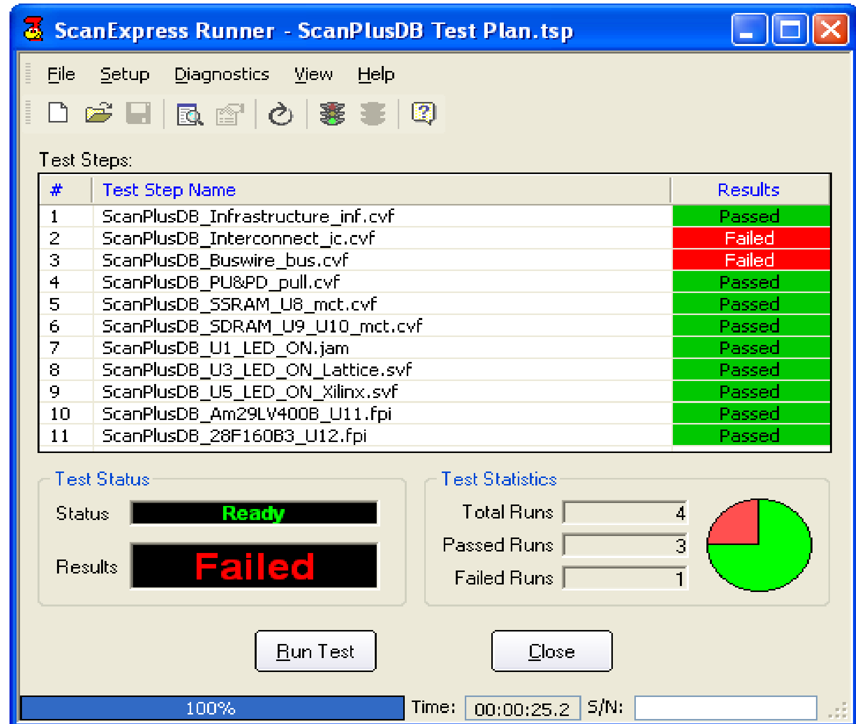

Figure 4. ScanExpress Runner Graphical User Interface

The ScanExpressTPG automatically generates test patterns that enable testing of boundary-scan chain integrity, PCB interconnects, buswires, and clusters including memories and FIFOs. These test vectors are then applied to the Unit Under Test through one of the Corelis boundary-scan controllers.

The ScanExpress comprehensive diagnostics package provides the location of the fault in the user's terms for netlist, IC name, and pin number. Figure 4 shows an example of the user interface seen when performing interconnect testing and in-system-programming; The ScanExpress Runner's fault diagnostics screen is shown in Figure 5.

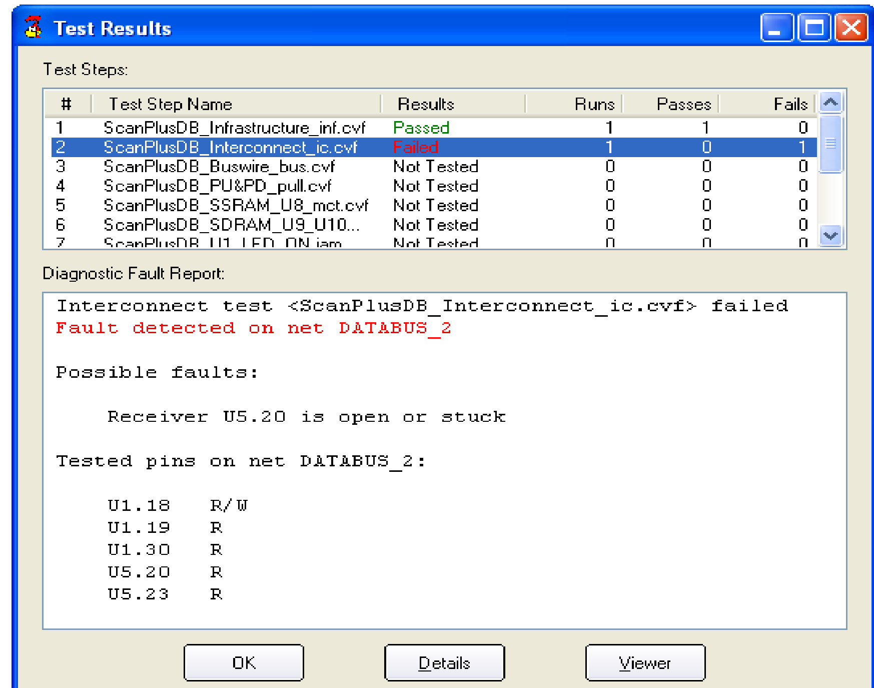

Figure 5. ScanExpress Runner Fault Diagnostics

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