

ScanExpress™

High-Volume Production Boundary-Scan Test and In-Circuit Programming System

- Concurrent (gang) testing and in-system programming of CPLDs and Flash devices for up to 1,024 boards
- User programmable sustained Test Clock (TCK) up to 80 MHz, in <2% increment per TAP, at effective throughput of 80Ghz
- Hardware comparison of expected patterns against observed results is done concurrently for each TAP
- Pre-power up test for shorts between power and ground lines on the UUT for each TAP
- TAP signals and GPIO discrete signals are individually programmable from 1.3V to 3.3V (5 volt tolerant)
- Direct Write signal for expediting Flash programming
- Support for monitoring Flash RDY/BSY
- Up to 30 feet of extended distance from the PC to the Pod, no TAP extenders are needed
- Automatic signal delay compensation for long cable lengths to the UUT
- 32-bit PCI bus interface supports high data transfer rates
- 16 bits of programmable parallel I/Os
- Plug and Play drivers for Windows 95/98/ME/NT/2000/XP
- Scalable architecture allows expansion of the system at incremental cost
- Fully compatible with Scan-Plus family of products



Overview

In the last few years, the use of boundary-scan has expanded beyond traditional board test applications into in-system programming of CPLDs, FPGAs, and Flash memories. These new applications require higher test and in-system programming throughputs.

Until now, boundary-scan testing and in-system programming was usually limited to a single board at a time. In high-volume production, users are now demanding higher throughput boundary-scan tools that will allow concurrent (often referred to as gang) testing and in-system programming of tens and hundreds of units under test.

The ScanExpress™ system was developed to address very high-speed boundary-scan applications and high-volume production. The ScanExpress™ family of products dramatically increases the test and in-system programming throughput by applying new, innovative, and pro-

prietary techniques tailored specifically for optimizing boundary-scan operating speed.

The ScanExpress™ architecture provides for concurrent testing and programming with practically unlimited scalability. For practical purposes, the software is configured to support up to 1024 UUTs.

General Description

Scan Express enables concurrent (gang) testing and in-system programming of CPLDs and Flash devices for up to 1,024 boards using a single PC and a single operator. What it means for the user is that if it takes 2 minutes to test and program a single board it will take also 2 minutes to program 120 boards, which is effectively 1 second per board. The ScanExpress™ System is composed of scalable components designed to work together to support various concurrent testing and in-system programming configurations.

The major elements of this system include:

- PCI-1149.1/Turbo™ boundary-scan controller
- ScanTAP-4 remote pod
- ScanTAP-8 remote pod
- ScanTAP-32 remote pod
- ScanHUB-16 boundary-scan expansion ports
- ScanExpress Runner software

The PCI-1149.1/Turbo™ boundary-scan controller card is the key element of the ScanExpress system. The PCI-1149.1/Turbo contains several performance enhancing functional elements aimed at increasing test vector and in-system programming throughput. The combination of these functional elements result in a very high data-scanning rate, which is completely decoupled from the PCI bus and the host computer.

The scan patterns, generated by the PCI-1149.1/Turbo™ controller, are then distributed to the target system either directly through the ScanTAP-4, ScanTAP-8 and ScanTAP-32 pods or via the ScanHUB-16 (see Figures 1, 2, 3. and 4).

The ScanTAP-4, ScanTAP-8 and ScanTAP-32 pods can apply test vectors and/or ISP patterns to target boards with a variety of JTAG chain topologies. In the simplest case, the ScanTAP-4, ScanTAP-8 and ScanTAP-32 will provide the interface between the PCI-1149.1/Turbo™ controller and a target system consisting of a single JTAG Test Access Port (TAP). This would be the case where the target system consists of one JTAG chain and its single associated TAP.

If the board under test consists of groups that include multiple devices, each with their own respective TAP, then the ScanTAP-4, ScanTAP-8 and ScanTAP-32 allow for test vectors to be applied to each of the target TAPs individually, one TAP at a time, or jointly to all of the TAPs. Figure 1 depicts such a configuration using the ScanTAP-4 pod.

Figure 2 depicts a case where the ScanTAP-4 is connected to four identical boards. Figure 3 shows a similar arrangement using a ScanTAP-8 or ScanTAP-32 pod. In all

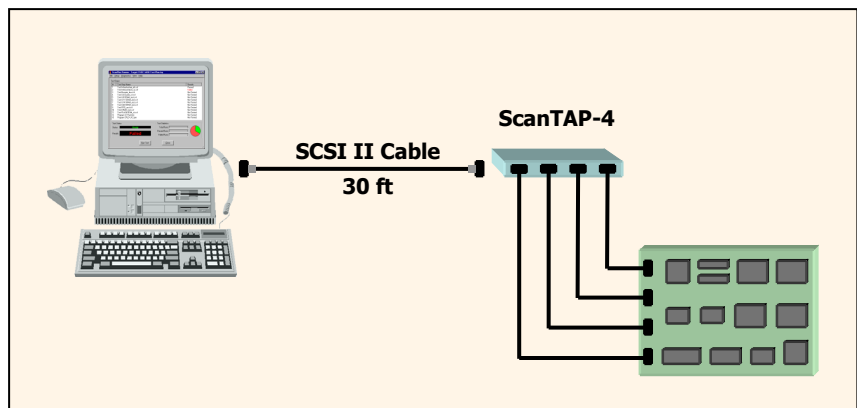


Figure 1. Connection to a single UUT with four TAPs

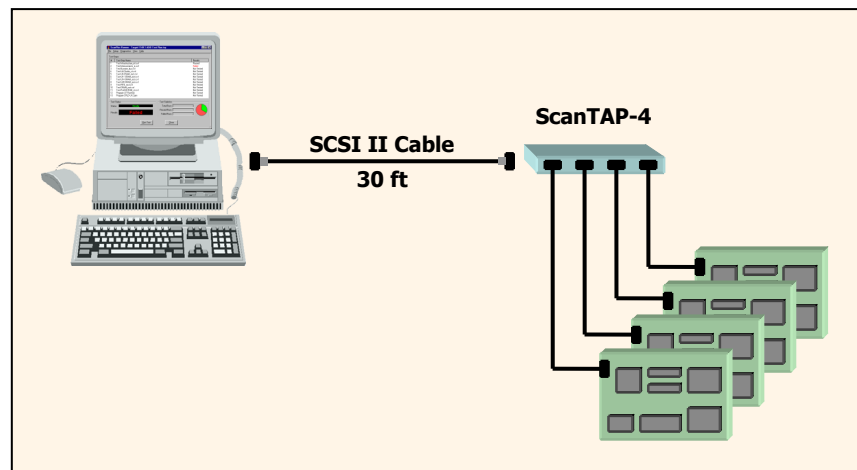


Figure 2. Connection to four UUTs with a single TAP each

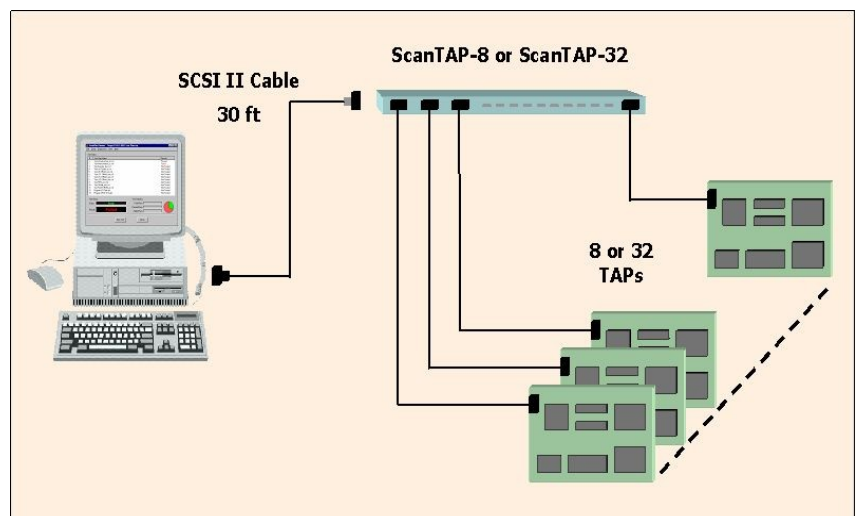


Figure 3. Connection to eight or thirty-two UUTs with a single TAP each

cases, the system can test and program the multiple target TAPs concurrently.

Note that the concept of concurrency here not only applies to the

simultaneous application of test vectors and ISP patterns to each board but also applies to the simultaneous verification of each individual board. A failure on any of the individual boards will be properly

logged and will not prohibit the continuation of testing on the remaining boards. The concurrent or gang mode of operation offers great performance increases when testing, in-system programming, and verifying multiple targets.

To accommodate for nearly unlimited scalability, Corelis provides the ScanHUB-16. Just like a network hub that fans a server's network connection to multiple clients on the LAN, the ScanHUB-16 fans out the PCI-1149.1/Turbo™ controller interface to multiple ScanTAP intelligent pods. The ScanHUB-16 connects the host boundary-scan controller to up to 16 ScanTAP intelligent pods, such as the ScanTAP-4, ScanTAP-8 or ScanTAP-32. As an example, a ScanHUB-16 with 16 ScanTAP-32 intelligent pods will enable the simultaneous testing and programming of up to 512 Target TAPs.

To further expand a system's TAP-scanning capability, the user can connect a second tier of ScanHUB-16 hubs to the expansion ports of the primary hub. This configuration fans out the controller to up to 256 (16×16) ScanTAP intelligent pods. Since each ScanTAP-32 pod can drive up to 32 TAPs, it enables the concurrent scanning of up to 8192 TAPs in total. Figure 4 shows standard configurations using the ScanHUB-16 in conjunction with multiple ScanTAP-4, ScanTAP-8 and ScanTAP-32 pods.

It should be noted that regardless of the configuration used, the actual connection to the target TAP remains the same and hence the definitions provided below apply equally well to all configuration options using either the ScanTAP-4, ScanTAP-8 or ScanTAP-32 (with or without the ScanHUB-16).

Programmable Clock

The system-wide TCK rate for all TAP ports is programmable under software control. A wide range of TCK frequencies can be achieved by using the on-board Phase-Locked-Loop (PLL) generation circuitry. The user is given the ability to select the desired TCK rate from a range of values up to 80MHz at resolution increments of less than 2%.

Should an external TCK timing ref-

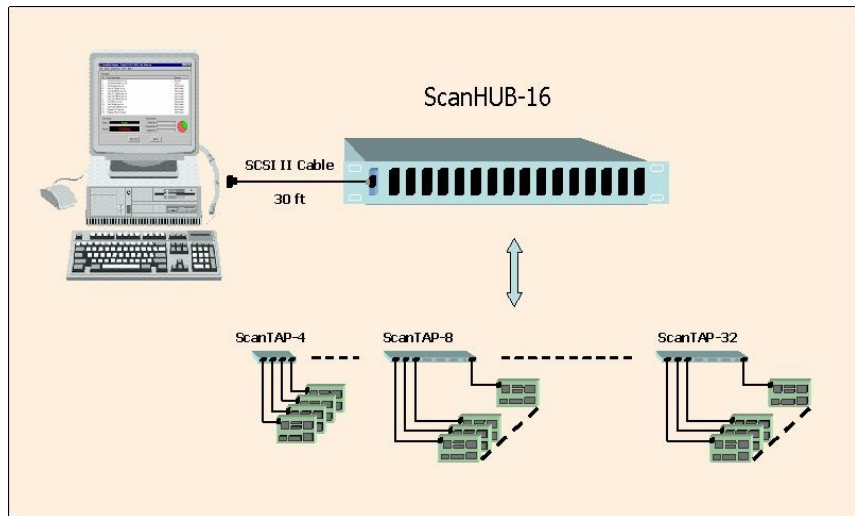


Figure 4. Connection to hundreds of UUTs with a single TAP each

erence be required for synchronization, or a user-unique frequency, an external SMB connector is provided.

Adjustable Low Voltage Outputs

The voltage level of the parallel I/O, the local TAP port, and each pod TAP is software programmable and can be set to any voltage between 1.3V and 3.3V (5V tolerant) in increments of 0.05V. The ports of the ScanTAP-4, ScanTAP-8 and ScanTAP-32 pods can also be slew rate (fast/slow) adjusted.

Scan Input Signal Delay Compensation

Automatic delay compensation is inserted within the signal paths. This feature solves the well-known problems associated with the combination of high TCK rates and remote target locations at extended distances.

Target Voltage Detection System

The Controller and its remote pod include analog-to-digital converters, which can measure connected power voltages from the target. Such voltages from two distinct target levels can be measured and compared against user-defined limits. This feature can provide detailed signal voltage checks at any stage of a test plan.

Automatic Detection of Target Power Shorts

With the target powered down, a well-regulated drive current with current limit can be momentarily applied to the target power bus. By measuring this current, the approximate load resistance can be calculated. This provides for the automatic detection of target power shorts, prior to applying power to the target unit.

Target Presence Detection Capabilities

The TAPs on the remote pod have a dedicated pin on the JTAG interface connector that can be used to detect the presence of the target board. The state of this signal can be monitored by software to detect both the presence of the target device as well as the proper insertion of the test cable.

Parallel Input/Output Port

The controller contains 16 parallel output signals. These output signals are organized into two 8 bit parallel ports. The 16 parallel outputs are implemented as tri-state logic that can be set to logical high, low, or high-impedance.

The output ports can be used to control various functions in the target system which cannot be controlled through boundary-scan operations.

These ports are useful for the test-

ing of target systems that incorporate components that are not compliant to IEEE Standard 1149.1.

In addition, each port of the pod controls 3 discrete output signals whose drive (totem-pole or open-collector) is configurable. Open-collector signals are often needed to drive reset and emulation signals.

Built-in Self-Test

The PCI-1149.1/Turbo™ has a built-in self-test capability. Logic has been provided at the local TAP connector to loop back data shifted out on TMS and TDO. Cooperative testing between the Controller and the pod has also been implemented to insure proper interface signal integrity. The Controller is a single function universal 32-bit 33MHz PCI device compliant with Revision 2.2 of the PCI Bus Specification. It is operational in either 5V or 3.3V interface signaling platforms. It is mapped to the memory space of the host system determined during system initialization.

ScanExpress Runner

ScanExpress Runner™ software is a powerful, yet easy to use, Test Executive that allows parallel testing and in-system programming up to 1,024 boards. An intuitive Graphical User Interface (GUI) allows the user to configure the ScanExpress Runner™ system to support practically any target configuration and JTAG chain topology.

ScanExpress Runner™ software then applies Boundary-Scan Test and ISP patterns to a Unit Under Test (UUT), reads back the responses, and provides comprehensive fault detection and isolation of the Boundary-Scan chain infrastructure, board interconnect, buswire, pullup/pulldown resistors, and clusters such as CPLDs, memories, FIFOs and other failures. Figure 5 depicts an example of the main window display.

Support for Third Party Test Executives

ScanExpress Runner is capable of executing boundary-scan tests and various In-System Programming (ISP) files from third party applications using DLLs or command line interface. Drivers for the popular National Instruments LabWin-

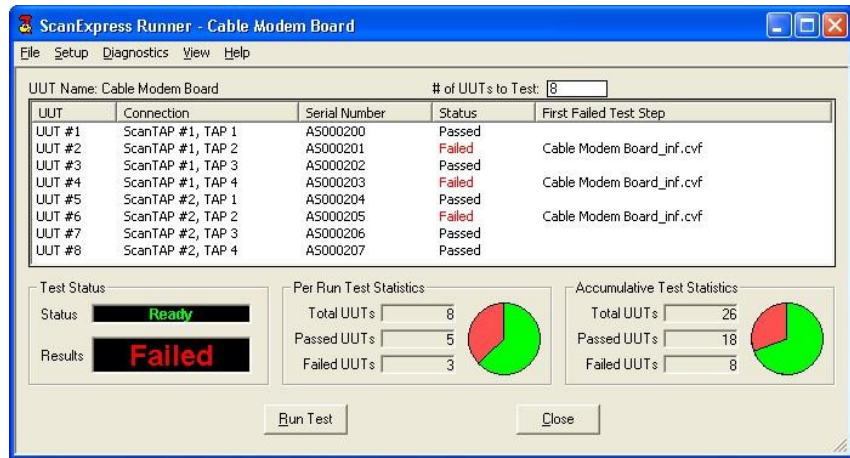


Figure 5. Connection to many of UUTs with a single TAP each

Pin	Signal Name	I/O	Description
1	TRST*	Out	Test Reset Output to UUT
3	TDI	Out	Test Data Output to UUT
5	TDO	In	Test Data Input from UUT
7	TMS	Out	Test Mode Select Output to UUT
9	TCK	Out	Test Clock Output to UUT
11	Write_Strobe* (GPIO1)	I/O	Write Strobe Output to UUT. Discrete I/O to/from UUT
13	GPIO2	I/O	Discrete I/O to/from UUT
15	Ready/Busy* (GPIO3)	I/O	Flash Ready/Busy* polling. Discrete I/O to/from UUT
17	VCC1	In	UUT Power Test Point 1
19	VCC2	In	UUT Power Test Point 2

Table 1- ScanTAP 20-pin Connector

Note: Direction specified is relative to pod. All other pins of the connector

dows/CVI, LabView, Agilent VEE test environments are provided.

ScanTAP-4, ScanTAP-8 and ScanTAP-32 Connectors

The ScanTAP-4, ScanTAP-8 and ScanTAP-32 contain four, eight and thirty-two, 20-pin TAP connectors respectively. Each of the ScanTAP target connectors has the same signals and the same pinout. Each connector is a shrouded header (0.100 x 0.100 in. spacing) with long ejectors that are compatible with

standard 20-pin IDC flat cable connectors (with strain relief). Note that only the first 10 pins are required for basic boundary-scan operation.

For Flash programming with external write or the Ready Busy signal, use the first 16 pins of the TAP. To build in support for power-to-ground short checking, use all 20 pins of the TAP.

Pins 17 and 19 of each ScanTAP connector can be used to sense that the target power pin is not shorted to GND. Up to 2 different power pins can be checked on each of the

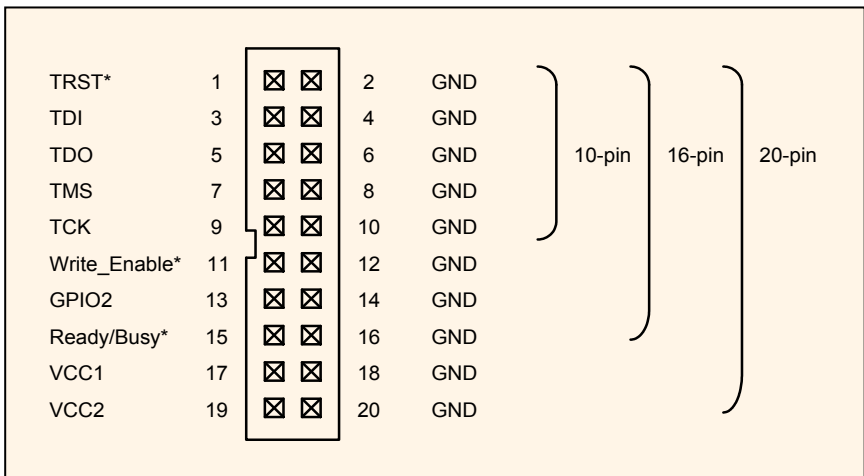
20-pin connectors of the ScanTAP unit.

The 3 GPIO signals are general-purpose output signals that are directly controlled by the Parallel I/O menu of ScanExpress Runner. The dual purpose Write_Strobe* (GPIO1) signal is used for Flash programming, and if used will override the Parallel Output (GPIO1) function. The dual purpose Ready/Busy* (GPIO3) signal is used for Flash programming, and if used will override the Parallel Output .

Ordering information

- ScanExpress-4
- ScanExpress-8
- ScanExpress-16
- ScanExpress-32
- ScanExpress-64

Contact Corelis for other configurations.



ScanTAP target connector pin assignments for various TAP cables

PCI-1149.1/Turbo Specifications:

Host Computer

CPU	Pentium II @ 266 MHz or better
Operating System	Windows 95/98/ME/NT/2000/XP

PCI Interface

Configuration	Plug and Play
Bus Width	32-bit
Memory Space	132 Mbytes
Signaling	5v or 3.3v (universal)

ScanTAP Interface

Maximum scanning data length	Unlimited
TCK frequency	User programmable sustained Test Clock (TCK) up to 80 MHz, in <2% increment per TAP

Physical

Board Outline Dimensions	3.875 in. × 6.75 in.
--------------------------	----------------------

I/O Connectors

Boundary-Scan Connector (P4)	68-pin SCSI II type (AMP p/n 787171 -7 or equivalent)
Parallel Input Port Connector (P1)	34-pin header (3M part no. 2534-6002UB or equivalent)
Parallel Output Port Connector (P2)	34-pin header (3M part no. 2534-6002UB or equivalent)

Power Requirements

From host expansion bus	5 Vdc @ 1.5 A maximum
-------------------------	-----------------------

Operating Environment

Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non-condensing

Storage Environment

Temperature	-40°C to 85°C
Relative Humidity	0% to 100%, non-condensing

ScanTAP Specifications:

PCI-1149.1/Turbo Interface

Host Connector	68-pin SCSI (AMP part no. 787171-7 or equivalent)
Host Cable Length	6 foot (standard) - Corelis P/N 15314 15 foot (optional) - Corelis P/N 15328 30 foot (optional) - Corelis P/N 15329

TAP Interface

Connectors	Four 20-pin shrouded headers, 0.1 in. × 0.1 in. spacing
Number of TAPs	4, 8 or 32
Maximum TCK frequency	80 MHz
Maximum scanning data length	unlimited
Programmable Interface Voltage	1.25 to 3.3 V in 0.05 V increments
Programmable TAPs	4, 8 or 32, each TAP can have its own programmable voltage settings
Signals DC characteristics	See Table 2

Power Short Test Pins

Power (Vcc) Sense Pins	Two per TAP (Vcc1, Vcc2)
Vcc Measurement Type	Short to GND detect; Voltage sensing, Target un-powered
Voltage Sense Resolution	8-bit ADC
Voltage Sense Accuracy	+/- 50 mV

Power Requirements

Supplied by controller

Operating Environment

Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non-condensing

Storage Environment

Temperature	-40°C to 85°C
Relative Humidity	0% to 100%, non-condensing

Symbol	Test Conditions	Limit Min	Limit Max	Units
V _{IH}	V _{DD} Adjust ≥ 2.5 V	2	V _{DD} + 0.5	V
	V _{DD} Adjust < 2.5 V	0.65 × V _{DD}	V _{DD} + 0.5	V
V _{IL}	V _{DD} Adjust ≥ 2.0		0.7	V
	V _{DD} Adjust ≤ 2.0		0.35 × V _{DD}	V
V _{OH}	I _{OH} = -2 mA	V _{DD} - 0.35		V
V _{OL}	I _{OL} = 2 mA		0.45	V
I _{OH}	V _{DD} = 1.65 - 1.95 V		-4	mA
I _{OL}	V _{DD} = 1.65 - 1.95 V		4	mA

Table 2- ScanTAP DC Characteristics

CORELIS

13100 Alondra Blvd.
Cerritos, California 90703
Tel: (562) 926-6727, Fax: (562) 404-6196
sales@corelis.com www.corelis.com

Windows®, WindowsNT®, WindowsXP®, Windows2000®, are trade-marks of Microsoft Inc.

ScanExpress, PCI-1149.1/Turbo are trademarks of Corelis Inc.

© Copyright 2005-2010 by Corelis Inc. All rights reserved.

CORELIS Inc., reserves the right to make changes in design or specification at any time without notice