

ScanPlus Chip Tester™

Boundary-Scan IC Tester with 2,040 I/O Pins

- Testing and verification of devices' internal SCAN logic and BiST
- BSDL file verification against actual silicon
- 2,040 I/O pins; each independently controlled as output, input, bi-directional, and tri-state
- 2,040 I/O pins are divided into 4 Voltage-Group blocks that are individually programmable from 1.8V to 3.3V
- Removable Device Under Test (DUT) fixture (optional) allows support for wide ranges of package types such as BGAs, TQFP, QFP, TSOP, etc.
- Test points are placed in 10 Pin-Group blocks of 204 pins. Each group can be bypassed to save scan time
- Compliant with IEEE-1149.1 and IEEE-1149.4
- Pre-power up test for shorts between power and ground lines on the DUT or its fixture
- Four analog test channels
- Three software programmable clock sources, up to 200 MHz
- Programmable Test Clock (TCK) up to 80 MHz
- 1 MByte on-board trace
- Four adjustable power supplies for the DUT
- Built-in self-test circuitry
- Optional cooling fan
- Separate power switch to DUT
- Product includes the high-performance PCI-1149.1/ Turbo™ boundary-scan test controller
- Fully compatible with ScanPlus™ family of products



Overview

As devices densities increased to millions of gates with I/O pin counts exceeding 2,000, the test and verification of silicon devices became complex, cumbersome, and expensive. The use of high density packages, such as BGA, with their diminishing physical access to the pins, required that device vendors incorporate boundary-scan technology into their chips.

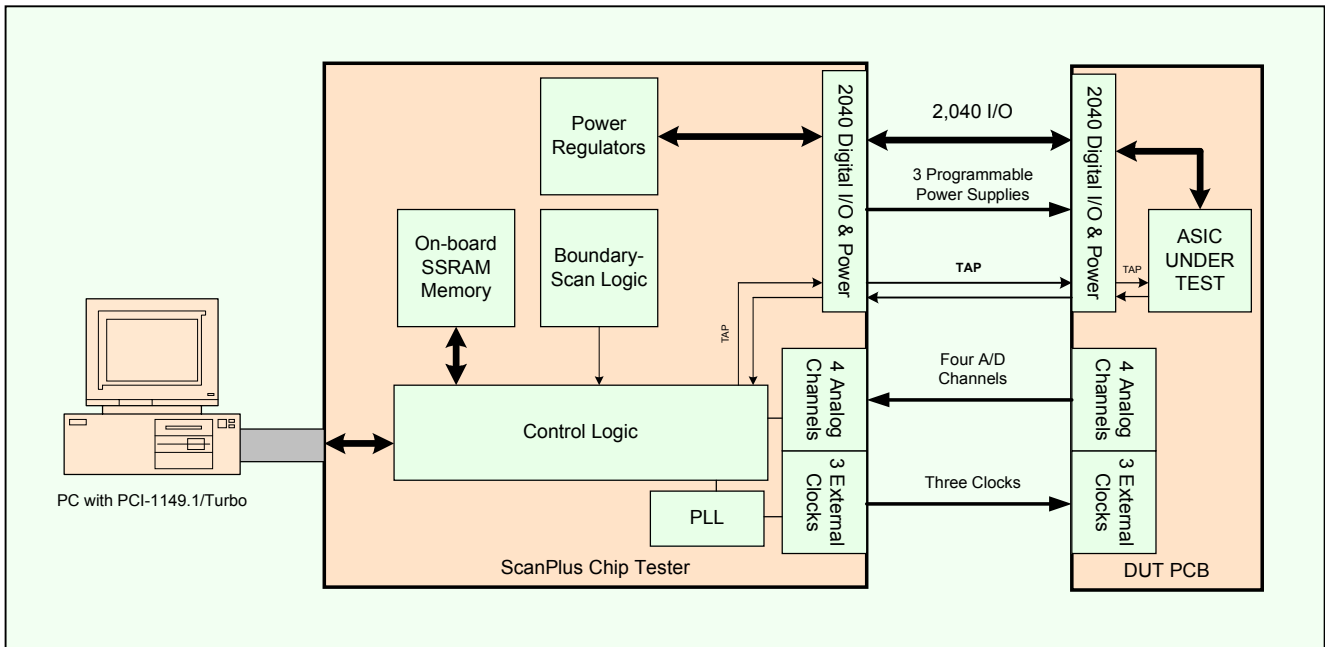
A critical factor in the success of testing devices and systems incorporating boundary-scan, is that the boundary-scan components are fully IEEE-1149.1 compliant and that their associated BSDL files accurately describe the test logic circuitry within the components.

Until now, very expensive semiconductor testers and test fixtures were used to perform device testing and boundary-scan verification functions. The ScanPlus Chip Tester can perform many of these same functions at a fraction of the cost, supporting components with up to 2040 I/O pins.

Applications that can be performed with the ScanPlus Chip Tester include:

- Verification that a Device Under Test (DUT) is fully compliant with the IEEE-1149.1 standard
- Verification that the BSDL file is compatible with, and correctly describes, the DUT
- Test internal functions and I/Os of the DUT
- Perform DFT test functions such as BiST
- Test Multi-Chip Modules and SOCs
- Perform structural tests of devices that include LogicVision's Embedded Test (ET) technology, using Corelis optional "LV Ready" software.
- Program embedded flash memories using Corelis ScanPlus Flash™ software

ScanPlus Chip Tester provides a powerful solution to the problem of boundary-scan testing and verification, even with the highest density



ScanPlus Chip Tester block diagram

and most complex semiconductor devices. Additionally, the ScanPlus Chip Tester can verify that an ASIC fully complies with the IEEE-1149.1 standard, verify BSDL files against the silicon, and runs at maximum TCK speeds.

Semiconductor manufacturers will benefit by having a single boundary-scan desk-top tester for multiple semiconductor devices, providing them with a low cost solution for customer support.

Custom ASIC designers can significantly reduce their time-to-market. The ScanPlus Chip Tester will shorten development cycles by providing an independent boundary-scan test station that allows functional testing and boundary-scan testing to be conducted in parallel.

Corelis provides a design service that will custom design the Device Under Test (DUT) interface board to the ScanPlus chip tester, or the user can design their own. (Please contact Corelis Sales regarding design services).

General Description

The ScanPlus Chip Tester uses boundary-scan compatible chips to add control and visibility to the Device Under Test (DUT). Functionally, the ScanPlus Chip Tester operates as a traditional "bed of nails" test

system, the difference being that access to the stimulus-and-response I/Os is achieved via Boundary-Scan instead of external nails. The application of stimulus-and-response patterns via Boundary-Scan greatly reduces the size and cost of the system, making it significantly smaller and less expensive when compared to traditional testers.

A PCI-1149.1/Turbo™ Controller connects to the ScanPlus Chip Tester with a high performance cable, available in lengths up to 30 feet for easy installation at remote locations.

The ScanPlus Chip Tester connects to the DUT inputs and outputs through high-density test connectors. The target DUT mounts to the ScanPlus Chip Tester on a separate PCB fixture using mating high-density test connectors. Test vectors that are driven by the boundary-scan controller (PCI-1149.1/Turbo), pass through the ScanPlus Chip Tester boundary-scan logic, then enter the DUT.

Each test pin is an **independently controlled** bi-directional signal, configurable as an input or output. The 2,040 I/O pins are divided into 4 Voltage-Group blocks that are individually programmable from 1.8V to 3.3V. To increase scan-vector throughput, the 2,040 I/O pins are divided into 10 Pin-Group blocks of 204 I/O signals. Each block of 204 I/O channels can

be bypassed (via the Boundary-Scan BYPASS command), thereby reducing the number of channels to fit the number of channels on the Device Under Test (DUT). Reducing the number of channels saves scanning time in time-critical test situations.

The ScanPlus Chip Tester contains several performance enhancing features aimed at providing a global solution for semiconductor testing. These features include:

- High test point count for large ASIC devices
- Independent control over each test pin
- Partial TAP chaining for smaller DUTs that do not require the full test point set
- 4 fully programmable voltage sources for powering the DUT
- On-board memory
- 4 analog A/D channels
- 3 fully programmable external clock sources
- Automatic self-test and an external fan connection for high power applications.

The various components of the ScanPlus Chip Tester are shown in the block diagram above.

Boundary-Scan I/O Pins

2040 individual boundary-scan I/O pins are provided with the ScanPlus Chip Tester. All Boundary-Scan controlled digital I/O lines on the ScanPlus Chip Tester are **independently controllable** and configurable as input or output. The ScanPlus Chip Tester is comprised of 10 boundary-scan devices, each having a total of 204 I/O. Each device may be bypassed using the Boundary-Scan BYPASS command to reduce the scan time for DUTs that do not require the full 2040 test points.

When not in use for boundary-scan purposes, all I/O pins are tri-stated fully isolating the ScanPlus Chip Tester from the DUT.

Programmable Power Supplies

Four independent power supplies are available on the ScanPlus Chip Tester for powering the DUT. Voltage levels are both manually and software adjustable between 1.8V and 3.3V.

Interface Connectors

ScanPlus Chip Tester utilizes Samtec high density connectors for the interface to the DUT interface board. Ten, 240-pin connectors are used, each providing contacts for up to 204 test signals. DUT fixture design requirements are provided with the ScanPlus Chip Tester for designing a compatible interface PCB. DUT fixtures may require less than 10 connectors if less than 2040 I/O pins are being tested.

Analog Test Channels

The ScanPlus Chip Tester provides 4 independent A/D channels that can be connected to analog pins on the DUT. The testing range for these pins is 0V-5V. The voltage values of these pins can be read by the ScanPlus Chip Tester software.

Programmable Clocks

Three clock sources are provided with the ScanPlus Chip Tester utilizing fully software programmable Phase-Locked-Loop (PLL) generation circuitry. The default frequencies for

ScanPlus Chip Tester Specifications:

Host Requirements

Boundary-Scan Controller	PCI-1149.1/Turbo
CPU	Pentium II @ 266 MHz or better
Operating System	Windows 95/98/ME/NT/2000/XP

DUT TAP Interface

DUT Standalone	80 MHz
Maximum TCK frequency	
EXTTEST Interconnection	45 MHz
Maximum TCK frequency	

Physical

Dimensions	12.20 in. × 11.05 in. x 4.00 in.
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PCI-1149.1/Turbo Interface

Host Connector	68-pin (AMP part no. 787171-7 or equivalent)
Host Cable Length	6' (standard) - Corelis P/N 15314 15' (optional) - Corelis P/N 15328 30' (optional) - Corelis P/N 15329

I/O Connectors

High Density Test Point	240-pin header (Samtec BTH-120-01-L-D-A)
External Clock	SMB Socket (Johnson Components 131-3701-261 or equivalent)
External Fan	3-Pin Header (Molex 22-11-2032 or equivalent)

Power Requirements

ATX	120VAC @ 6A maximum
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Operating Environment

Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non-condensing

Storage Environment

Temperature	-40°C to 85°C
Relative Humidity	0% to 100%, non-condensing

these channels are 25 MHz, 150 MHz and 200 MHz. Channel 1 is fully programmable from 1 to 100 MHz, while the other two channels are programmable to frequencies up to 200 MHz. SMB connectors are provided for external clock sources.

buffer. The memory is software programmable and its content can be read by the host software.

On-Board Memory

A one Megabyte memory module is provided with the ScanPlus Chip Tester that can be used as a trace

Device Under Test (DUT) Interface Board

The DUT is situated on a special custom board. The user can add any special circuitry required for the DUT, such as local oscillators, reset circuitry, and voltage reference sources.

ScanPlus Chip Tester provides the following features through its unique mechanical interface:

- Mounting and Dismounting of the interface board is accomplished via an easy-to-use, positive locking mechanism
- No special tools are required for insertion or extraction of the interface board
- Mechanical keying provides easy and safe alignment for DUT board insertion
- Mounting kit hardware is available from Corelis
- FPGA board will be available from Corelis for users who want to first test their ASIC design inside a standard FPGA before or during ASIC fabrication

Built-in Self-Test

The ScanPlus Chip Tester includes a built-in self-test that verifies all required voltage levels. A ScanPlus Chip Tester self-test daughter card is provided with the module to verify that all pins are functioning correctly.

ScanPlus Family of Products

The ScanPlus Chip Tester is software compatible with the ScanPlus family of IEEE-1149.1 test and in-system programming products.

Ordering Information

ScanPlus Chip Tester (P/N 10315) that includes:

- ScanPlus Chip Tester
- PCI-1149.1/Turbo Boundary-Scan controller card (P/N 10267A) including cable
- ScanPlus Chip Tester User's Manual
- ScanPlus Chip Tester self-test daughter card

Optional Accessories

- External Fan
- Clock Connector Cable – SMB to SMB
- Custom daughter card that meets your chips needs.

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