

“We combine exceptional ease of use with advanced technical innovation”

ScanExpress Merge™ System-Level Test Productivity Tool

- ❑ Complies with IEEE Std 1149.1
- ❑ Merges board-level netlists and test files into a system-level netlist and test data
- ❑ Automatically merges the harness between connectors residing on various boards
- ❑ Maintains system hierarchy of original sub-assembly, net, device, and pin names in diagnostic reports
- ❑ Enables automatic testing of complex systems that include boards and/or backplanes with daughter boards, Multi-chip Modules (MCM), and various sub-systems
- ❑ Supports all types of boundary-scan testing, including infrastructure, interconnect, clusters, memories, and FIFOs
- ❑ All details are saved in a Merge Plan for easy recall and regeneration
- ❑ 32-bit Windows® applications with an easy-to-use Graphical User Interface
- ❑ Easy-to-use built-in step-by-step wizard
- ❑ Built-in support for Corelis ScanIO™ and ScanDIMM™ parallel I/O modules
- ❑ Automatically generates connection lists for mated connectors and generates suggested wire lists for connectors that are selected by the user to connect to Corelis ScanIO modules
- ❑ Compatible with all other Corelis ScanExpress™ products

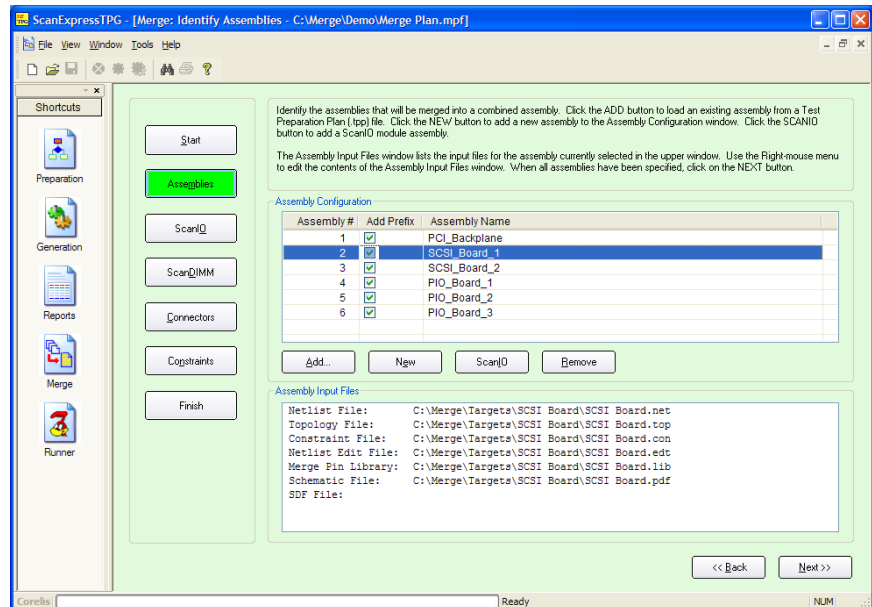


Figure 1. ScanExpress Merge GUI

Introduction

Until now, boundary-scan testing has been primarily used as a complete test and programming solution for single printed circuit board (PCB) assemblies. Now the use of boundary-scan testing can be easily extended to test systems that consist of multiple PCBs, treating them as a single, combined unit.

ScanExpress Merge™ can be used to combine multiple target assemblies into a single boundary-scan compatible target system. ScanExpress Merge has many applications, including:

1. Motherboard and Daughter card(s) assembly testing
2. Target assembly and ScanIO Digital Tester module testing
3. Multiple card chassis testing
4. Gang testing of multiple cards

ScanExpress Merge can be used in a similar manner for any system topology. By providing the netlist and data files for each of the individ-

ual assemblies, ScanExpress Merge will combine them into a single set of files. The merged files can then be used to generate test vectors for the entire system as a whole.

By default, ScanExpress Merge will add a prefix to the names of items that are associated with each assembly such as net names, device identifiers, etc. This allows the user to uniquely identify each assembly within the combined system and to properly diagnose faults when the complete system is tested.

ScanExpress Merge is compatible with both ScanExpressTPG™ and ScanExpress Flash Generator™ programs and supports all of the various test generation files. Furthermore, ScanExpress Merge will automatically merge the connector pins of the assemblies and combine the nets on both sides of the connectors. This feature is very useful in motherboard-daughter card applications.

Overview

ScanExpress Merge is a software application that facilitates the generation of boundary-scan test vectors for multiple targets. The ScanExpress Merge application can be viewed as a pre-processor for ScanExpressTPG. It merges the data files for multiple individual targets, referred to as assemblies, into a combined set of files that can be used for vector generation by ScanExpressTPG.

In a typical application, the user can use ScanExpressTPG to generate tests for each of the boards in a system independently. After having generated and tested each board in a stand-alone mode, the user can run ScanExpress Merge and combine all of the test generation files into a single combined file set.

One common application for ScanExpress Merge is the testing of Main and Daughter boards together as a combined assembly as depicted in Figure 2. Testing the three assemblies together and the interconnects between them, increases the test coverage of the assemblies as a whole.

Another common application is a backplane with several boards plugged in, as shown in Figure 3. By supplying the data files for the backplane and the plug-in boards, ScanExpress Merge will combine these into a single set of data files for testing of all of the assemblies together.

Graphical User Interface

The ScanExpress Merge software is integrated into the ScanExpressTPG development environment. ScanExpress Merge provides an interactive Graphical User Interface (GUI) as shown in Figure 1, which guides the user with the entry and configuration of assemblies in the merge plan. Once all assembly information has been defined, a single click of the FINISH button initiates the merging of the test data files.

To further simplify operations, ScanExpress Merge automatically adds a prefix to the names of items that are associated with each assembly such as net names, device identifiers, etc. This allows the user to uniquely

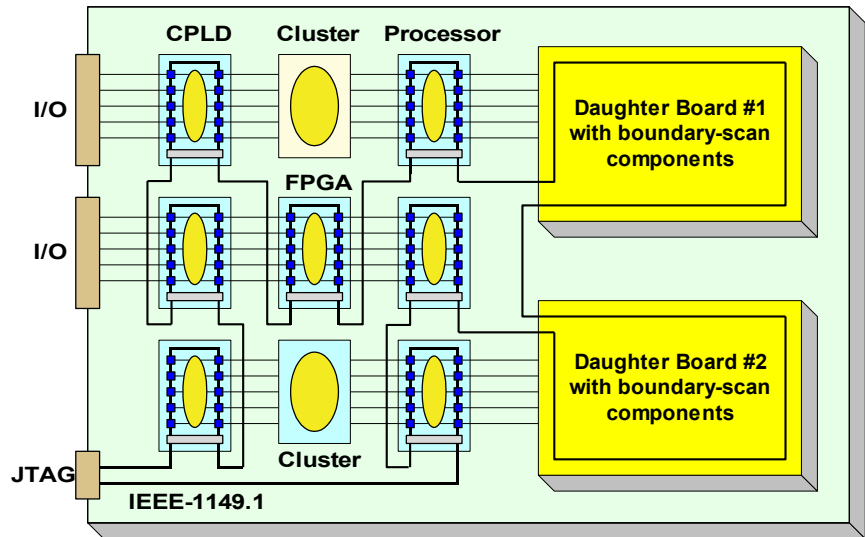


Figure 2. Testing a Main board and two Daughter boards

identify each assembly within the combined system and to properly diagnose faults when the complete system is tested. The default prefix is optional for each of the merged assemblies and can be changed by the user. ScanExpress Merge generates a unified set of input files that are compatible with Corelis' ScanExpressTPG Test Program Generator. ScanExpressTPG will automatically process the merged assemblies and generate test vectors for the entire combined system, thereby extending boundary-scan testing and programming to the system level.

ScanDIMM and ScanIO Module Support

ScanExpress Merge also automates the process of testing board IOs and

traces that are connected to DIMM memory sockets and ScanIO connectors. ScanExpress Merge combines the data of the board and the data of the ScanIO and ScanDIMM parallel IO modules into a single set of merged input files that are compatible with ScanExpressTPG. Adding support for boundary-scan parallel IO modules saves time by eliminating the need to describe the connections between the PCB connectors and the modules.

Connector Wire List Generation

When connecting boards using a connector that plugs directly into a mating connector, ScanExpress Merge automatically finds and connects the relevant nets on both sides of the connectors. The user is only

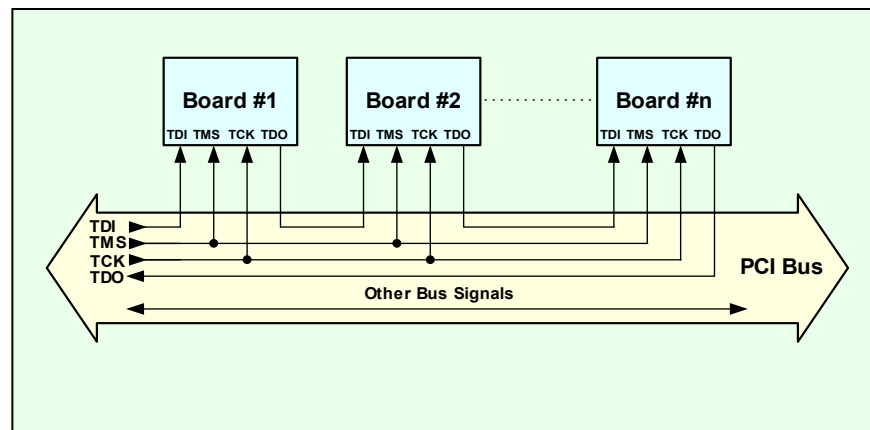


Figure 3 Testing a PCI backplane and PCI cards

required to specify which connector(s) are mated. This feature is very useful when using daughter cards that plug into motherboards or cards that plug into a backplane. In addition, ScanExpress Merge automatically generates connection lists for mated connectors and generates suggested wire lists for connectors that are selected by the user to connect to Corelis ScanIO modules. This allows an engineer to follow ScanExpress Merge's recommended connection list rather than having to prepare the ScanIO-to-UUT connection list manually.

ScanIO Modules

Corelis family of ScanIO modules turn any IEEE-std-1149.1 boundary-scan controller into a powerful digital boundary-scan tester. The ScanIO family of products use boundary-scan gate arrays to add control and visibility to connectors, traces, and logic that otherwise can not be tested using traditional boundary-scan techniques. The ScanIO products, when combined with a boundary-scan controller, operate as a traditional "bed-of-nails" tester except access to the stimulus and response I/O's is achieved via boundary-scan.

A listing of available ScanIO modules is provided below:

- ScanIO-300LV
- ScanPCI™
- ScanDIMMs

ScanIO-300LV

The ScanIO-300LV digital I/O module provides a low cost alternative to traditional stimulus-and-response digital testing. Through the use of boundary-scan technology, the ScanIO-300LV module provides a total of 300 fully bidirectional test channels with virtually unlimited memory depth per pin.

Each I/O line is independently controlled and can be individually configured as an input or output. During testing, the programming and control of the test channels is automatically performed by the ScanPlus™/ScanExpress tools without any user intervention. The voltage level of the I/O and JTAG interfaces is programmable from 1.25 to 3.3V and sup-



Figure 4. ScanIO-300LV Boundary-Scan Controlled Digital I/O Module

ports either single ended or low voltage differential (LVDS) signaling.

Multiple ScanIO-300LV modules can be cascaded in series providing a sufficient number of pins for almost any digital test environment.

By using single or multiple ScanIO-300LV modules, existing Automatic Test Pattern Generators (ATPGs) can be used to test non-scannable elements such as connectors, cables, and devices not incorporating boundary-scan. The ScanIO-300LV connects to the UUT inputs and out-

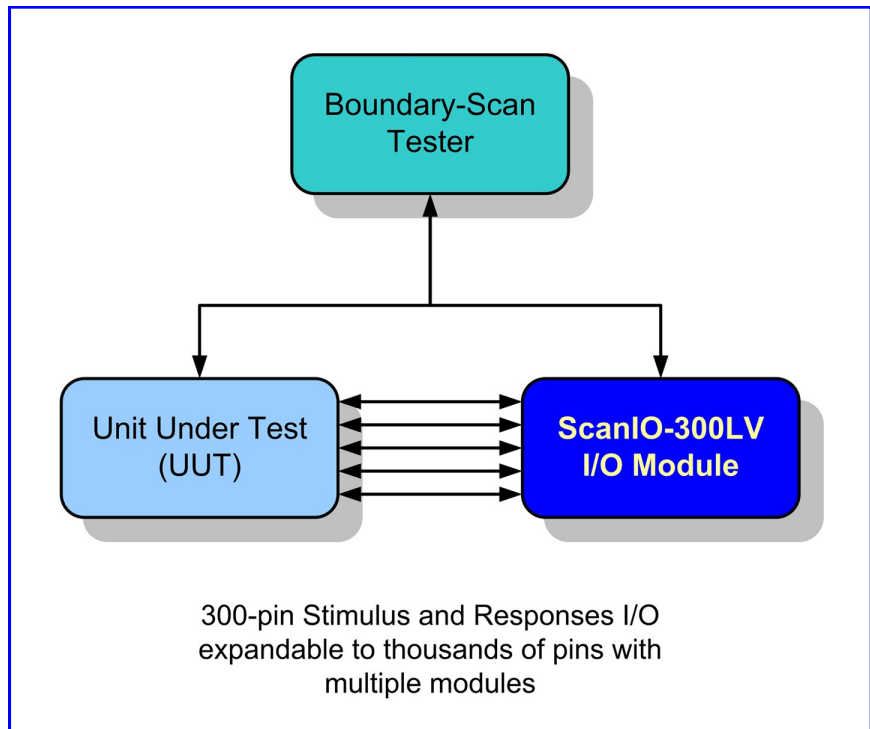


Figure 5. ScanIO-300LV Boundary-Scan Controlled Digital I/O Module

puts with standard flat-cables that can optionally be terminated with test probes. Figure 5 shows a typical test configuration using the ScanIO-300LV module and a boundary-scan controller such as the Corelis PCI-1149.1/Turbo™ or NetUSB-1149.1™. The scan chain originates from the scan controller, goes through the ScanIO-300LV, then through the UUT and back to the controller. Thus, a single scan chain can test not only all scannable elements on the UUT, but also the edge connector or other non-scannable elements.

For complete information on the ScanIO-300LV, please refer to the detailed data sheet for this product.

ScanDIMM

The ScanDIMM Digital Tester modules (shown in Figure 6) are easy to use tools for interconnect testing of DIMM sockets. Through the use of boundary-scan technology, the ScanDIMM Tester provides fully bi-directional test signals. A boundary-scan Test Access Port (TAP) connects to a host computer which provides virtually unlimited memory depth for testing each of the DIMM socket(s) pins. DIMM sockets are often used for Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) and other types of memories and the ScanDIMM offers an accurate and easy to use mechanical and electrical solution for testing connections to the DIMM socket(s). Support is available for a number of DIMM formats including 184-pin DIMM, 168-pin DIMM, 144-pin SODIMM, and 200-pin SODIMM.

For complete information on the ScanDIMMs, please refer to the detailed data sheet for this product.

ScanPCI™

The ScanPCI™ boundary-scan PCI and Compact PCI Card Tester provides a convenient method to test PCI and Compact PCI boards and their card-edge connectors. The ScanPCI adds boundary-scan control and visibility to PCI and Compact PCI connectors that would otherwise not be testable or require expensive wiring adapter harnesses. The ScanPCI is depicted in Figure 7.

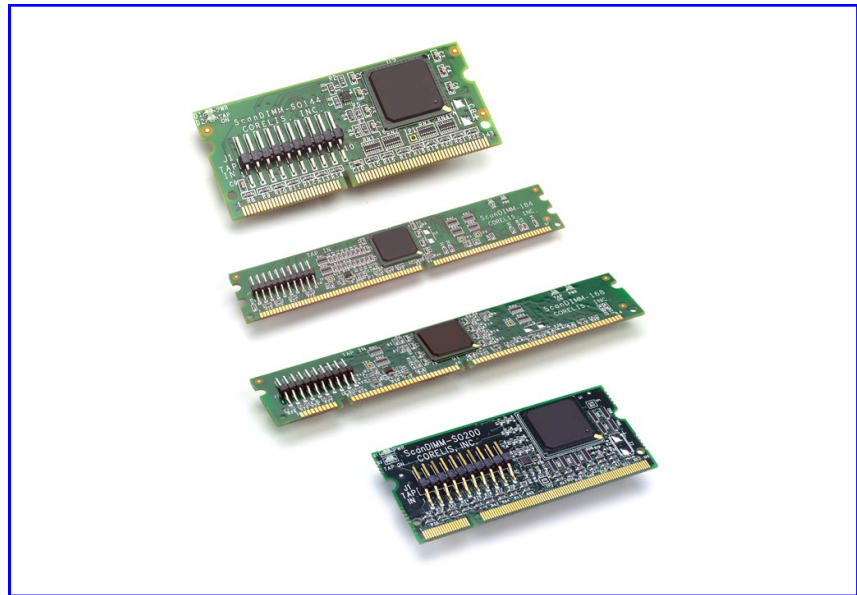


Figure 6. ScanDIMM Boundary-Scan DIMM Socket Tester

Even for those PCI and Compact PCI cards that have been designed with boundary-scan testing in mind, the circuitry between the PCI or Compact PCI card edge itself and the PCI interface devices, which typically have JTAG capability, is usually not fully boundary-scan testable. The Corelis ScanPCI provides a way to quickly and easily access these hard to reach connections

and increase the boundary-scan test coverage of the Unit Under Test (UUT).

The ScanPCI interfaces with a UUT that is either a 3.3V, 5V, or a Universal voltage device.

Refer to the detailed data sheet of the ScanPCI for additional information.

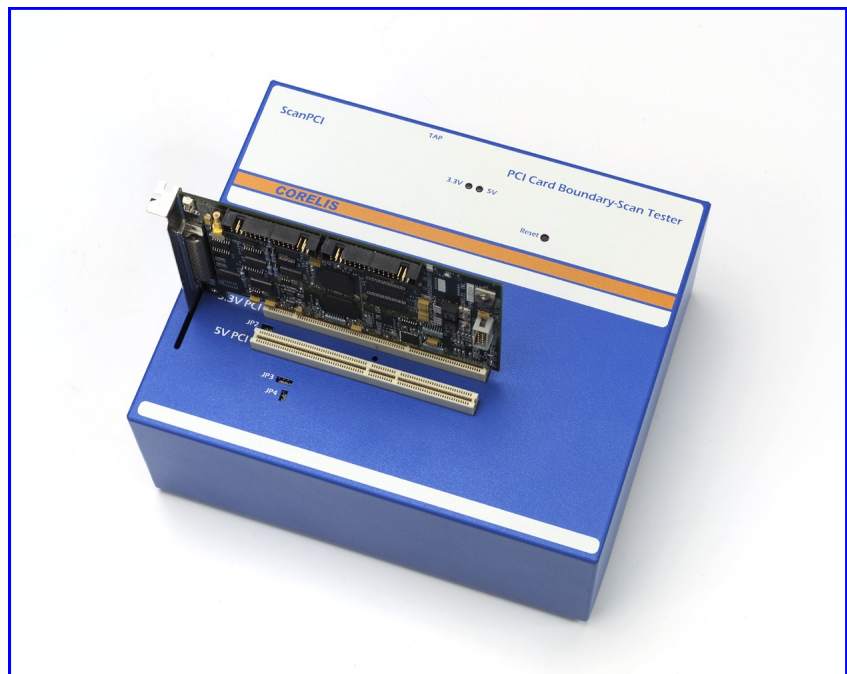


Figure 7. ScanPCI PCI and Compact PCI Card Boundary-Scan Tester

ScanExpress Family

Corelis has a complete family of boundary-scan test and in-system-programming tools. The complete Corelis family of ScanExpress tools provides a user with the ability to perform comprehensive boundary-scan interconnect testing and in-system-programming of CPLDs and Flash devices on their board. Software is available for infrastructure and interconnect testing of both boards and systems. Boundary-scan defect testing is particularly useful for finding stuck at, opens, shorts, and bridging faults when using BGA components or other fine pitch, difficult to probe, packages.

The ScanExpress family of tools includes an automatic boundary-scan Test Pattern Generator (ScanExpressTPG), boundary-scan test execution and in-system-programming software (ScanPlus Runner™), and a boundary-scan interactive debugger. The ScanExpressTPG automatically generates test patterns that enable testing of boundary-scan chain integrity, PCB interconnects, buswires, and clusters including memories and FIFOs. These test vectors are then applied to the Unit Under Test through one of the Corelis boundary-scan controllers. The ScanExpress comprehensive diagnostics package provides the location of the fault in terms of netlist, IC name, and pin number. Figure 8 shows an example of the user interface seen when performing interconnect testing and in-system-programming. The ScanPlus Runner's fault diagnostics screen is shown in Figure 9.

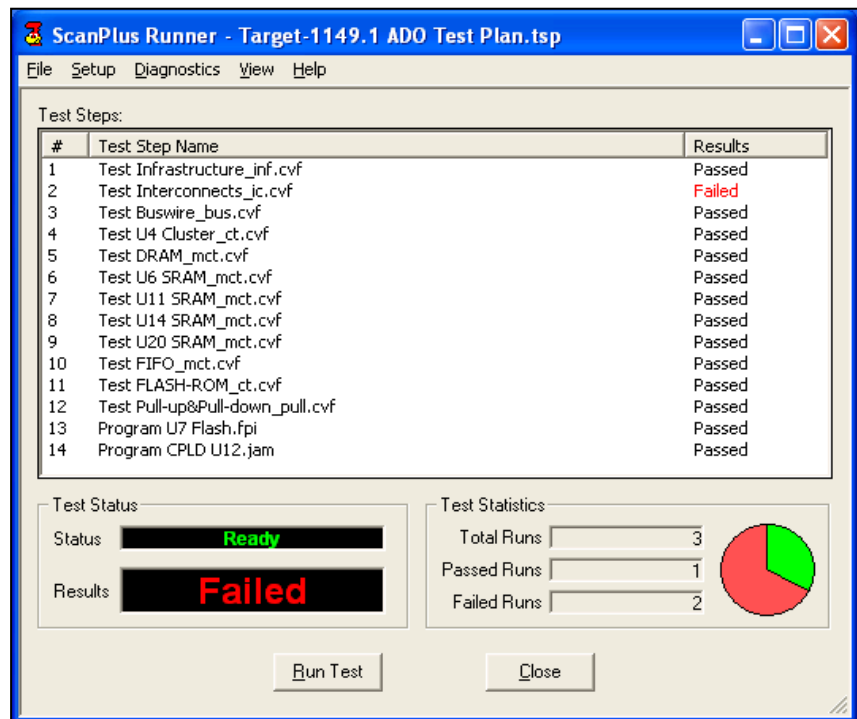


Figure 8. ScanPlus Runner Main Window

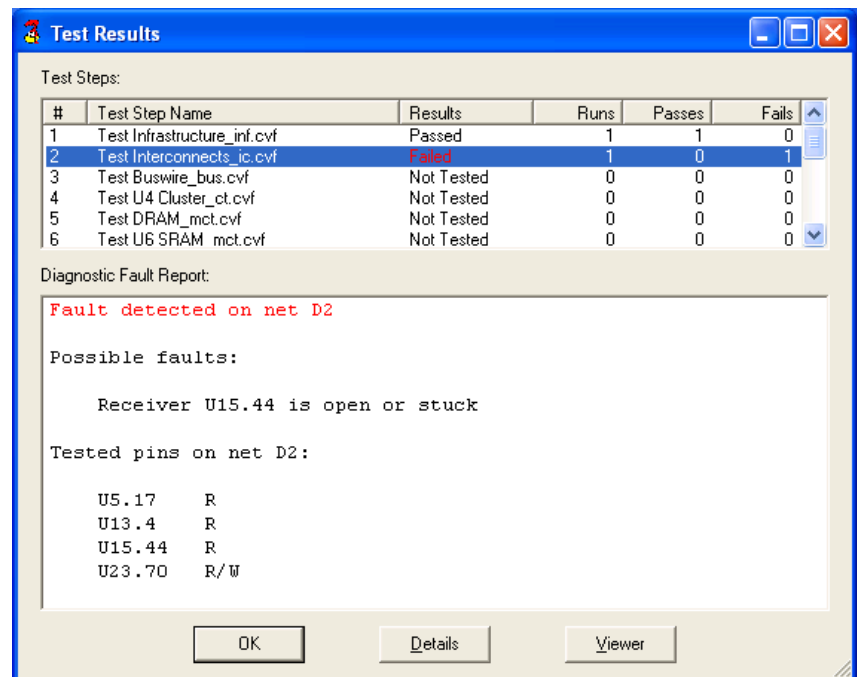


Figure 9. Fault Detection and Advanced Diagnostics

System Requirements

The ScanExpress software packages are Microsoft Windows 32-bit applications. The PC on which the ScanExpress Software will be installed should meet the following minimum hardware and software requirements:

- Microsoft Windows 2000 or XP installed
- CD-ROM drive
- Pentium processor or higher
- 512 Megabytes of RAM
- 200 Megabytes of free hard disk space for all ScanExpress applications (individual applications can be excluded at time of install if not required)
- Display adapter supporting at least 800x600 resolution and 256 colors. Recommended resolution is 1280 x 1024 or higher.

A standard 25-pin parallel port or USB port. The ScanExpress software is protected with a hardware key attached to the printer port or USB port. The hardware key has a pass through which will not affect the operation of a printer. Optional soft-key and network license are available.

Ordering Information

Model Numbers:

- ScanExpress Merge

CORELIS

13100 Alondra Blvd.
Cerritos, California 90703
Tel: (562) 926-6727, Fax: (562) 404-6196
sales@corelis.com www.corelis.com

Windows®, WindowsXP®, and Windows2000® are trademarks of Microsoft Inc.

ScanExpress Merge, ScanIO, ScanDIMM, ScanExpress, ScanExpressTPG, ScanExpress Flash, ScanPCI, ScanPlus, PCI-1149.1/Turbo, NetUSB-1149.1/E, and ScanPlus Runner are trademarks of Corelis Inc.

© Copyright 2006-2010 by Corelis Inc. All rights reserved.

CORELIS Inc., reserves the right to make changes in design or specification at any time without notice