

## ScanPCI™

### PCI and Compact PCI Card Boundary-Scan Tester

- Enables boundary-scan (JTAG) testing of PCI and Compact PCI (cPCI) cards
- Extends Boundary-scan Test Coverage and provides easy access to PCI and Compact PCI edge connectors
- Provides test coverage for the hard-to-test traces between the PCI or Compact PCI edge connectors and devices connected to them
- Supports JTAG TAP connection through the PCI or Compact PCI bus interface or directly to UUT
- Multi-layer, low noise PCB construction with ground and power planes
- Fully compatible JTAG/IEEE 1149.1 Test Access Port (TAP)
- Supports 3.3V, 5V and universal I/O PCI cards
- Internal ATX style power supply included
- Power indicator LEDs
- Selectable PCI bus clock speed
- Reset switch for generating reset to UUT
- Software supplied contains BSDL and other files for automatic test pattern generation with ScanPCI
- Compatible with the optional ScanPlus™ family of products for testing and in-system programming of Flash memories and CPLDs

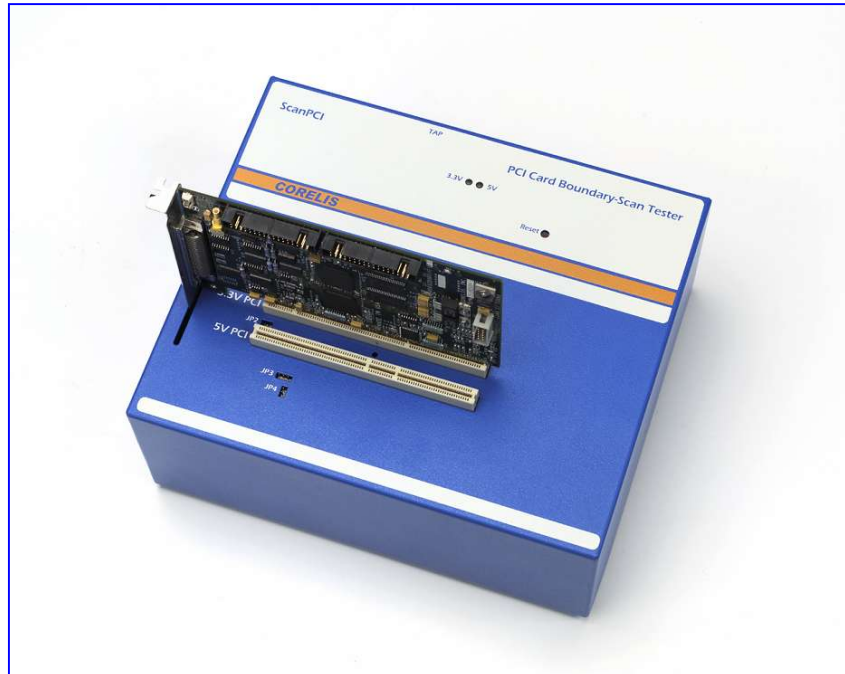


Figure 1. ScanPCI Module

#### Introduction

The PCI Local Bus is a high performance, 32-bit or 64-bit bus with multiplexed address and data lines. The bus is intended for use as an interconnect mechanism between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems.

Even for those PCI and Compact PCI cards that have been designed with boundary-scan testing in mind, the area between the PCI or Compact PCI card edge itself and the PCI interface devices, which typically have JTAG capability, is not fully boundary-scan testable. The Corelis ScanPCI™ provides a way to quickly and easily access these hard to reach connections and increase the boundary-scan test coverage of the Unit Under Test (UUT).

#### ScanPCI Overview

The ScanPCI boundary-scan based PCI and Compact PCI Card Tester provides a convenient method to test PCI and Compact PCI card-edge connectors. The ScanPCI is designed to add boundary-scan control and visibility to PCI and Compact PCI connectors that would otherwise be untestable or require expensive wiring adapter harnesses.

The ScanPCI is capable of interfacing with a UUT that is either a 3.3V, 5V, or a Universal voltage device.

The following features are included in the ScanPCI:

- Internal ATX style power supply
- 5V 32-bit/64-bit PCI Connector Socket
- 3.3V 32-bit/64-bit PCI Connector Socket
- Corelis Compatible PCI TAP

Connector

- Disk containing netlist, BSDL files, and software for integration with Corelis ScanPlus tools.
- Optional Compact PCI interface module

### Connecting the UUT to the ScanPCI

The ScanPCI has two separate sockets on the top side of the instrument. The socket labeled "3.3V PCI" is for both 3.3 volt and universal voltage PCI and Compact PCI cards. The socket labeled "5V PCI" is exclusively for 5 volt PCI devices.

If a target UUT is designed to be a universal or 3.3 volt PCI or Compact PCI card, then it is installed in the ScanPCI connector labeled "3.3V PCI". If the UUT is designed to use 5 volts, then it is installed in the ScanPCI connector labeled "5V PCI". During testing, the ScanPCI will apply the appropriate power to the UUT using its internal ATX style power supply.

### Connecting the JTAG TAP of the UUT to the Boundary-Scan Controller

There are two methods of connecting the JTAG TAP of the UUT to the boundary-scan controller. The first method is used when the JTAG signals on the UUT are brought to an external header. The second method is used when the JTAG TAP signals of the UUT are routed to the PCI or Compact PCI card-edge connector.

#### Target UUT TAP connection on an External Header:

When the JTAG TAP signals from the target UUT are brought to a header, the recommended and most common approach is to use an external ScanTAP-4 Intelligent Pod to chain the Target UUT with the ScanPCI module. One side of the ScanTAP-4 Pod interfaces with the boundary-scan controller in the host test system and the other side of the Pod interfaces with both the ScanPCI and the target UUT. In this case, the user simply connects TAP1 from the pod to the TAP connector on the target UUT and TAP2

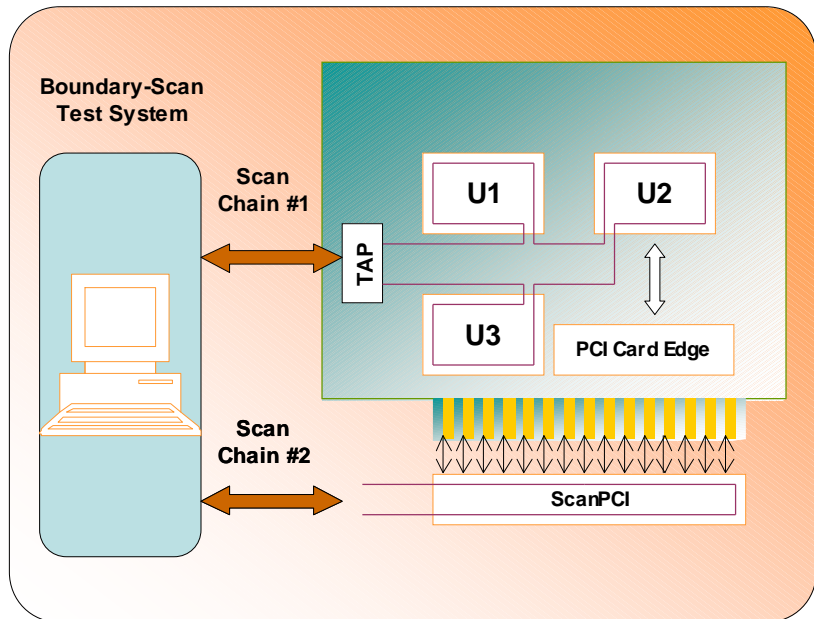


Figure 2. Target TAP signals routed to an external header

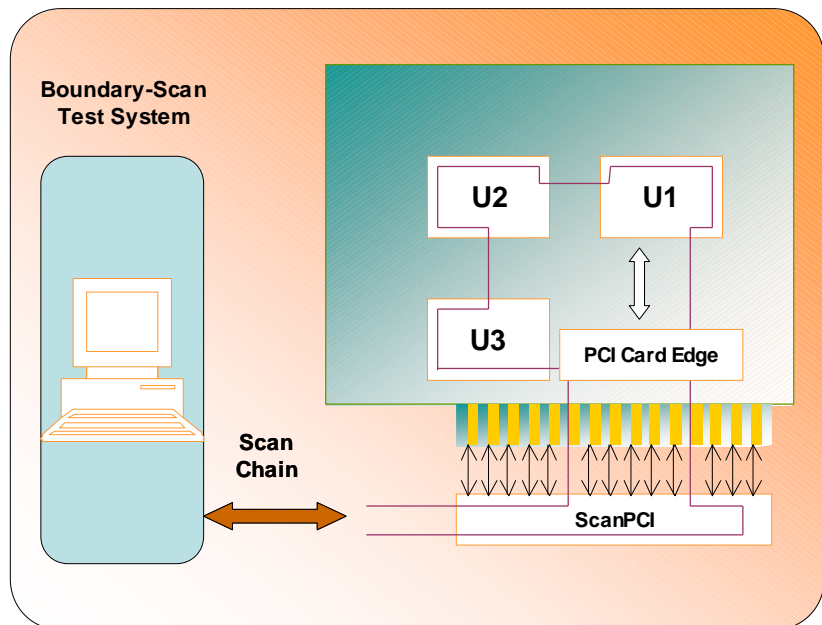


Figure 3. Target TAP signals routed to the PCI card-edge

from the pod to the ScanPCI connector labeled "TAP". Figure 2 shows the TAP connections for the Target UUT on TAP1 (Scan Chain #1) and the ScanPCI module on TAP2 (Scan Chain #2).

#### Target UUT TAP Connections on the PCI Card-edge Connector:

The ScanPCI also supports the connection of the TAP signals from the ScanPCI to the target UUT over the PCI or Compact PCI card-edge connector. For this case, connect the

10-pin cable from the boundary-scan controller (via the ScanTAP-4 pod) to the ScanPCI TAP connector. The connection list for the TAP signals on the card-edge connector are defined by the PCI and Compact PCI specifications and must be followed.

Figure 3 shows a block diagram for the TAP connection from the ScanPCI module to the target UUT over the PCI card-edge connector.

## Generating Test Vectors

The ScanPCI integrates easily with a boundary-scan test plan. When a PCI or Compact PCI card is installed in a ScanPCI socket, the socket behaves like a boundary-scan component.

Once the PCI or Compact PCI card is plugged into the socket of the ScanPCI, the boundary-scan test system will automatically test the card-edge connector.

To generate test vectors, a user simply copies the appropriate BSDL file from the supplied disk to the current ScanPlusTPG design directory, then adds the ScanPCI module to the topology file and regenerates the test vectors.

## Self-Test

The ScanPCI module is supplied with self-test vectors to verify proper operation of the module prior to testing the UUT. The self-test vectors are used with ScanPlus Runner to perform a ScanPCI chain integrity test to verify proper communication between the boundary-scan controller, ScanTAP-4 remote pod (if present), and the target UUT.

## Target TAP Connector

The TAP connector on the user's target should accommodate a standard 10-pin flat cable. Below is the top view of the target 10 pin connector header (0.100" x 0.100") spacing. Two such connectors are listed below, one with a latch ejector, and one without. 3M part number 30310-6002HB, (straight header with center notch, and 3M part number 3793-5602UG, (latch/ejector straight header with notch).

## Specifications

### Size

10.5" x 9.0" x 4.5"

### Status Indicators

Power ON/OFF indicator

### Logic Levels

Outputs CMOS (3.3V, 5V tolerant)  
Inputs TTL

### Max TCK clock frequency

10 MHz

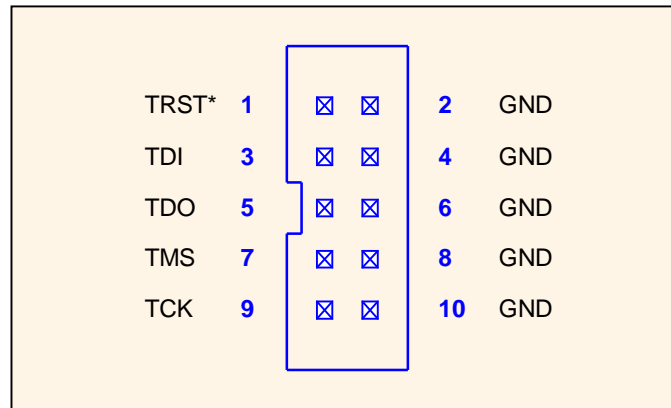


Figure 4. Standard TAP Connector

Symbol	Conditions	MIN	MAX	UNIT
$V_{IH}$	High Level Input Voltage	1.7	5.75	V
$V_{IL}$	Low Level Input Voltage	-0.5	0.8	V
$V_{OH}$	$I_{OH} = -8\text{mA DC}$	2.4		V
	$I_{OH} = -0.1\text{mA DC}$	$V_{CC} - 3.1$		V
$V_{OL}$	$I_{OL} = 8\text{mA DC}$		0.45	V
	$I_{OL} = 0.1\text{mA DC}$		0.2	V
$I_I$	$V_I = V_{CC}$ or GND	-10	10	$\mu\text{A}$
$I_{OZ}$	$V_o = V_{CC}$ or GND	-10	10	$\mu\text{A}$

Figure 5. I/O and TAP Signals Characteristics

## I/O Connectors

JTAG Connector (TAP) 10-pin IDC (3M part no. 3793-6302 or equivalent).

## JTAG Interface

IEEE-1149.1 compliant interface

## Power

Internal ATX style power supply

## Operating environment

Temperature 0 to 55C. Relative humidity 10% to 90%, non condensing

## Storage environment

Temperature -40 to +85C

## Ordering Information

- ScanPCI Hardware, Corelis P/N 10328
- ScanPCI User's manual
- Disk containing netlist, BSDL files, and software for integration with Corelis ScanPlus tools.
- Optional Compact PCI Interface Module, Corelis P/N 10350

## ScanPlus Family

Corelis has a complete family of boundary-scan test and in-system-programming tools. The complete Corelis' family of ScanPlus tools provides a user with the ability to perform comprehensive boundary-

scan interconnect testing and in-system-programming of CPLDs, FPGAs, and Flash memory devices.

Software is available for infrastructure and interconnects testing of both boards and systems. Boundary-scan defect testing is particularly useful for finding stuck-at faults, opens, shorts, and bridging faults when using BGA components or other fine pitch, difficult to probe, packages.

The ScanPlus family of tools includes an automatic boundary-scan Scan Test Pattern Generator (ScanPlusTPG™), boundary-scan test execution and in-system-programming software (ScanPlus Runner™), and a boundary-scan interactive debugger.

ScanPlusTPG automatically generates test patterns that enable testing of boundary-scan chain integrity, PCB interconnects, buswires, and clusters including memories and FIFOs. These test vectors are then applied to the Unit Under Test through one of the Corelis boundary-scan controllers.

The ScanPlus comprehensive diagnostics package provides the location of the fault in the user's terms for netlist, IC name, and pin number. Figure 6 shows an example of the user interface seen when performing interconnect testing and in-system-programming; The ScanPlus Runner's fault diagnostics screen is shown in Figure 7.

## ScanExpress

Until now, boundary-scan testing and in-system programming was usually limited to a single board at a time. In high-volume production, users are now demanding higher throughput boundary-scan tools that will allow concurrent (often referred to as gang) testing and in-system programming of tens and hundreds of units under test.

ScanExpress™ was developed to address very high-speed boundary-scan applications and high-volume production. ScanExpress dramatically increases the test and in-system programming throughput by applying new, innovative, and proprietary techniques tailored specifically for optimizing boundary-scan operating speed.

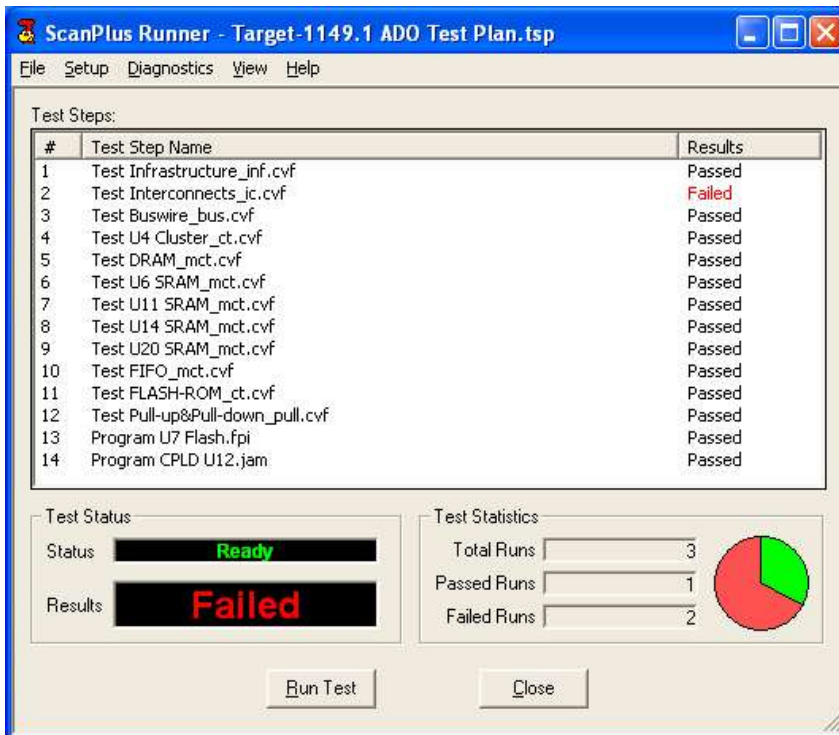


Figure 6. ScanPlus Runner Graphical User Interface

ScanExpress enables concurrent (gang) testing and in-system programming of CPLDs and Flash devices for up to 1,024 boards using a single PC and a single operator. What this means for the user is that if it takes 2 minutes to test and program a single board then it will also take only 2 minutes to program 120 boards, which is effectively 1 second per board.

ScanExpress is comprised of scalable components designed to work together to support various concurrent testing and in-system programming configurations.

For complete information on ScanPlus Runner and ScanExpress, please refer to the detailed data sheet for these products.

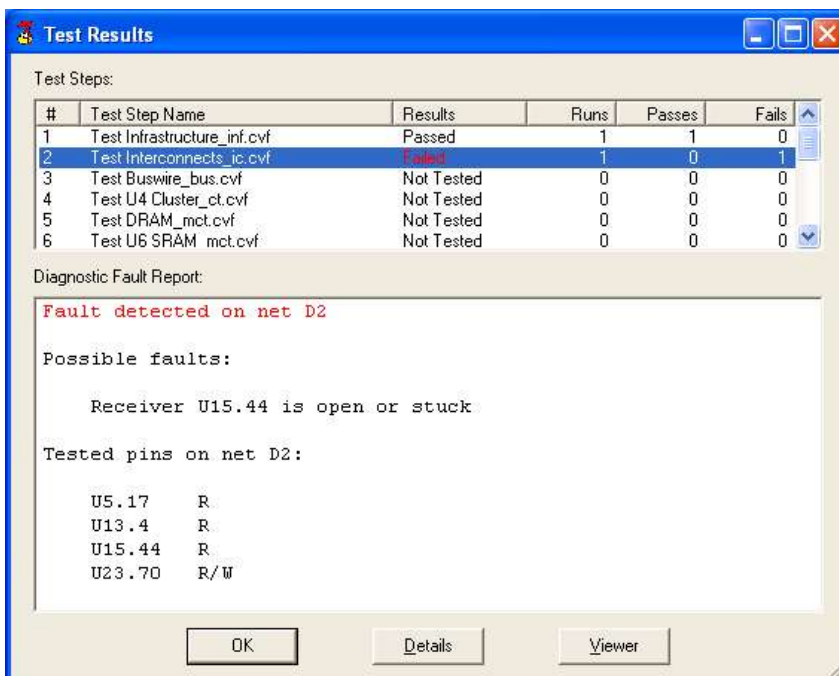


Figure 7. ScanPlus Runner Fault Diagnostics

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