



UniSTAC II / J for IOP321 In-Circuit Emulator



- ❑ Supports Intel® IOP321 I/O Processors
- ❑ Supports CPU maximum clock speed
- ❑ ARM/Thumb state code debugging
- ❑ Hardware breakpoint can be set for address/data/status conditions (2 instruction BPs, 2 data BPs)
- ❑ Unlimited software breakpoints
- ❑ Branch trace capability
- ❑ Performance measurement
- ❑ Flash memory write capability
- ❑ View/modify internal registers
- ❑ Watchpoint®, powerful C/C++ high level language debugger, is included
- ❑ USB and LAN host interfaces supported for high-speed communication with host computer

Specifications

Target CPU	Intel® IOP321 I/O Processor, 80200, 80219 Processor
Target Vcc	Vcc= 3.0 ~ 3.6 VDC (3.3 V output signals from ICE)
Target Connection	EmbeddedICE interface (14-pin header), Multi-ICE interface (20-pin header)
Memory and I/O	Entire space is available to user except that 2Kbytes is required for monitor
Interrupts	Both internal and external interrupts are available to user
Breakpoints and Break Options	<p>Execution instruction address, memory access, data breakpoints can be specified. Max 4 Hardware breakpoints available (*1):</p> <ul style="list-style-type: none"> • 2 instruction execution breakpoints • 2 data access breakpoints <p>Software breakpoint options:</p> <ul style="list-style-type: none"> • Unlimited software breakpoints (not valid in ROM area) <p>Other break options:</p> <ul style="list-style-type: none"> • Forced break from Debug Monitor
Branch Trace	Records Branch instruction history, and trace instructions until break
Performance Analyzer	Measures cache hit rate
Flash Memory	Download the program from the debugger to target external Flash memory

Note *1: When 2 execution breakpoints are in use, some limitations apply during Software BP, Step Over, Step Out, Come To.

Configuration

The UniSTAC™ II/J IOP321 provides a high level of software debugging from your PC/AT or notebook computer. It is a development tool for designs containing an Intel® IOP321 I/O Processor with a JTAG interface for debugging. The UniSTAC-II/J IOP321 ICE connects to a JTAG port connector on the target.

Hardware

A UniSTAC-II/J IOP321 emulation system consists of the IOP321 Probe Set with USB host interface (optional LAN interface available).

Probe Set

The Probe Set consists of the IOP321 Probe Unit, JTAG Cable A, JTAG Cable B, and AC Adapter.

USB and LAN Interface

USB and LAN interface can be used for high-speed communication between the host PC and ICE.

Software

Watchpoint®, a high-level language debugger for Windows® 98/Me/NT/2000/XP, is included with the IOP321 Probe Set.

Media:

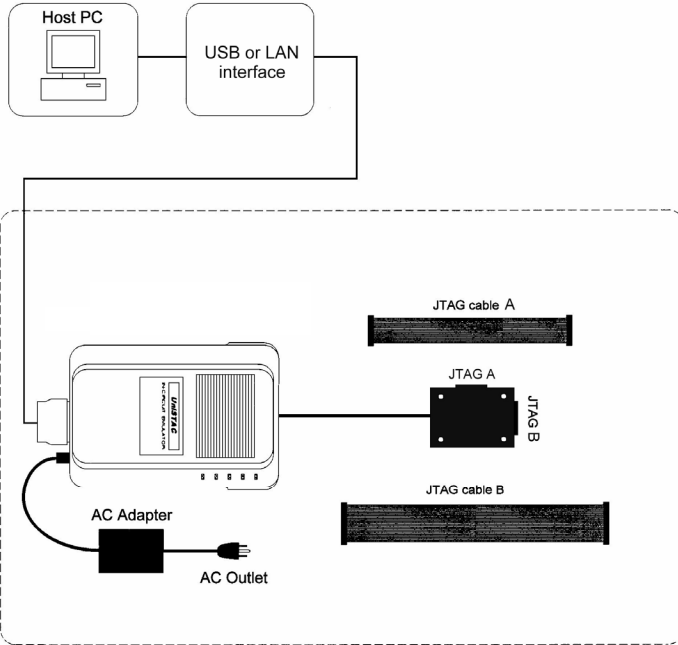
CD-ROM

Supported OS

Linux

Supported Tool Chains:

Watchpoint supports the following compilers:
ARM ADS, RealView

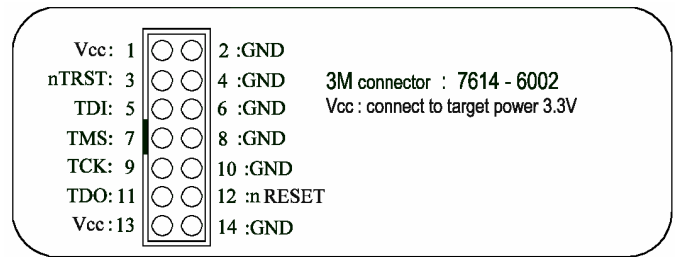


UniSTAC II/J IOP321 ICE System

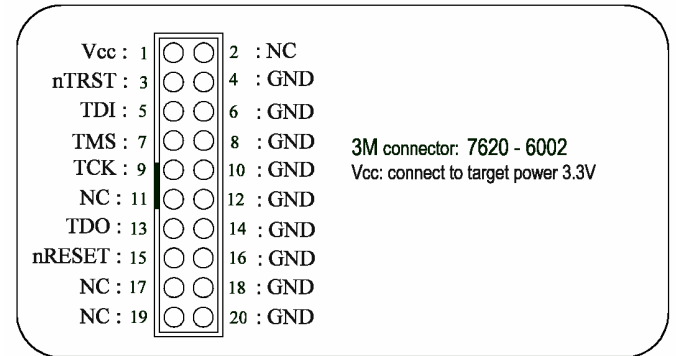
System requirements for Watchpoint® Debugger:

OS: Windows98/Me/NT/2000/XP
Memory: 32 Mbyte (64 Mbyte recommended)
Hard Disk: 20 Mbyte for installation

Target JTAG ICE Connection



EmbeddedICE interface (JTAG A) connection



Multi-ICE interface (JTAG B) connection

Selection Guide&Ordering Information

Host PC	Host Interface	Branch Trace	UniSTAC II / J for IOP321
DOS/V or laptop (IBM PC/AT or compatible)	USB interface	None	Product Code: UT15020E Product Name: US2-IOP321-JL-U-E
	USB interface	Yes	Product Code: UT15000E Product Name: US2-IOP321-J-U-E
	LAN/USB interface (LAN is recommended)	Yes	Product Code: UT15001E Product Name: US2-IOP321-J-UT-E

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