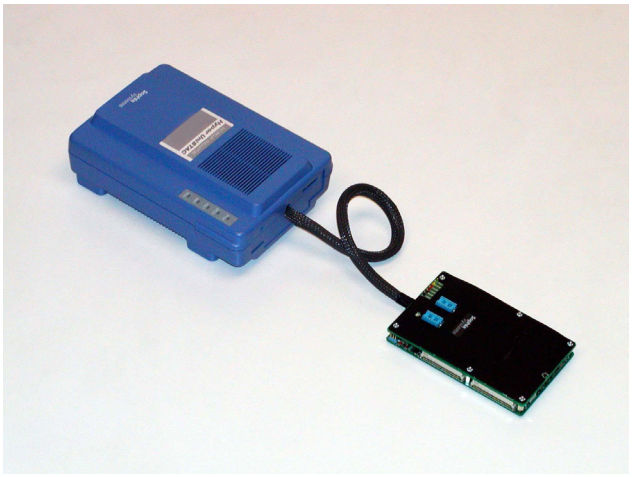
Sophia systems™

Product Brief

Ver 1.11

HyperSTAC™ H8S/2633R In-Circuit Emulator



- Supports Renesas Technology H8S/2633R microcontroller
- Supports 2 ~ 28 MHz clock speed
- Optional probe end adapters are available to support different MCU packages
- Internal access trace capability
- View and modify internal peripheral
- Unlimited software breakpoints
- **Flash ROM** download capability
- 4M Emulation Memory as standard
- **USB** and **LAN** host interfaces supported for high-speed communication with host computer
- Watchpoint®, a powerful high-level language debugger for Windows®, provides common user interface for all Sophia Systems emulators
  (USB: Windows98/Me/2000/XP)
  (TCP/IP: Windows98/Me/NT/2000/XP)
- IBM PC/AT or compatible, NEC PC98, and Notebook PC

Specifications

Target CPU	H8S/2223/25/27/28, H8S/2233/35/37/38, H8S/2621/22/23, H8S/2631/32/33/36/38/39/41/ 42/43/43F/45/46/47/48 series, H8S/2633R, 2695
Emulator CPU	H8S/2633 EVA chip, PGA401-pin
Memory and I/O	Entire space is available to user.
Packages	FP-128, TFP-120, TFP-100G, FP-144
Interrupts	Both internal and external interrupts are available for real-time MCU execution.
CPU Clock	Maximum 28 MHz
Target Voltage	3V ~ 5V
Breakpoints and Break options	Execution address can be specified
ICE Environment Settings	Enable/disable bus cycle time-out Enable/disable target control signals: RESET, NMI, STBY, BREQ
Reset	Reset the MCU during program execution
Emulation Memory	Internal ROM 512K, 64K internal RAM, 4 Mbytes SRAM is available for emulation memory as standard. Memory block can be mapped to SYSTEM/USER with Write-protect, Access-protect
Flash Memory	Download to target external Flash memory

Real-time Trace **(64K clock cycles branch trace storage capacity)**	-Store trace address, data, status, external control signal (Delay count: Max 65536 cycles) **Real-time Trace Mode**: **Free run-** Continuously records Trace data **Point area**- Max 5 points **And-** Triggers when all of the points are satisfied (any sequence) **Or-** Triggers when one of the points is satisfied. **Sequential-** Triggers on sequential levels **Sampling-** Records specific trigger cycles **Trigger Point Conditions:** The following conditions can be specified when defining trigger points: **Code Fetch** **Address:** Specify a memory address or address range. (Maskable) **Data:** Specify a data value (Maskable) **Data size:** 2 types of data size can be specified **Status:** CPU status(5 types) can be specified. **Others:** Write protect error, Time out, Time stamp
Bus Monitor	Monitor a specific block of memory data bus in real-time
Coverage Performance Analyzer	The following measurements can be performed **Profile**: Measures the frequency of the program cycle, or the module cycle within the respected address spaces. **Coverage**: Measures the ratio of instruction execution, access data address spaces. **Performance**: Measures the time of the program execution cycles, the function execution time.

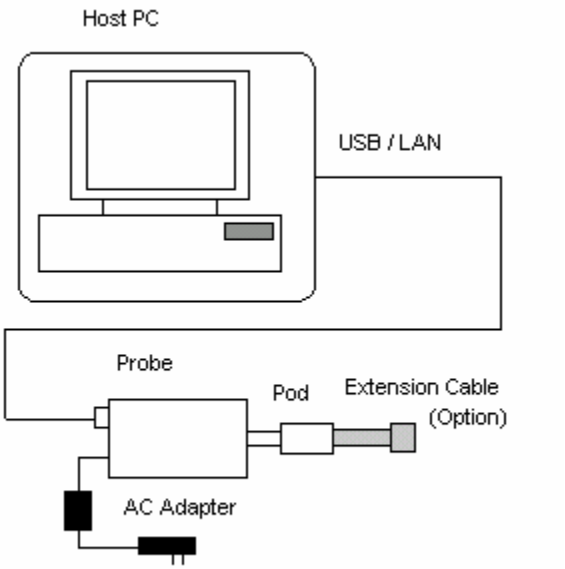
Note: The specification is subject to change at any time.

Configuration

The HyperSTAC is the latest state of the art emulator, which connects directly to your PC/AT or notebook computer and provides a high level of software debugging for embedded system development.

Hardware

The HyperSTAC H8S/2633R Emulation System consists of the H8S/2633R Probe Set and with USB host interface or LAN interface as an option.



Software

Watchpoint®, a high-level language debugger for Windows® , is included with the H8S/2633R Probe Set.

Media:

CD-ROM

Supported Tool Chains:

Watchpoint supports the following compiler and assemblers:

Supported Compiler

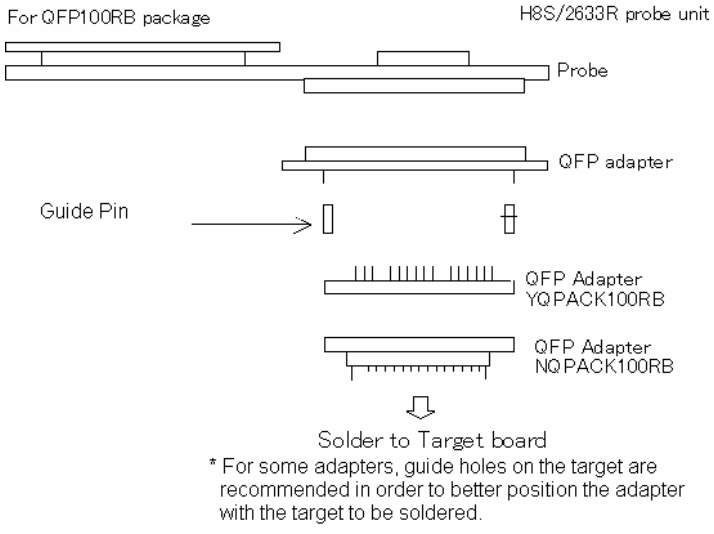
Renesas	H8S family compiler/assembler
IAR	ICC H8S/2633

Supported OS

NORTI 3.4

Hi 8 – 2600

Target Connection



* For some adapters, guide holes on the target are recommended in order to better position the adapter with the target to be soldered.

Ordering Information

Part No.	*Description*
HY45000E	Probe Set, HyperSTAC H8S/2633R with USB interface, and Watchpoint® H8S/2633R debugger
HY45001E	Probe Set, HyperSTAC H8S/2633R with USB & LAN interface, and Watchpoint® H8S/2633R debugger
CS2242E	Extension Cable(Option)

Probe End Adapters

CPU	Package	Required adapters(Option)
H8S/2633,2633R, 2695	FP-128	CS2245M 2633-PB-QF128-AD CS2245B YQPACK128RD CS2245C NQPACK128RD
	TFP-120	CS2245N 2633-PB-QF120-AD CS2243B YQPACK120SE CS2245Y NQPACK120SE
H8S/2623 series	FP-100B	CS2245V H8S/2623 ADAPTER KIT CS2231B YQPACK100SD CS2231C NQPACK100SD or CS2245V H8S/2623 ADAPTER KIT CS2645B H8S/2633-PB-FP100B-AD YY9000H IC149-100-*25-B5 (Yamaichi)
H8S/2636,38,39	FP-128	CS2645A HY-2636/46-PB-QF128-AD CS2245B YQPACK128RD CS2245C NQPACK128RD

CPU	Package	Required adapters(Option)
H8S/2237	FP/TFP-100B	CS2245R 2633-PB-QF100SD-AD CS2231B YQPACK100SD CS2231C NQPACK100SD
	FP-100A	CS2245Q 2633-PB-QF100RB-AD CS2360X YQPACK100RB CS2360Y NQPACK100RB
H8S/2227	TFP-100G	CS2245P 2633-PB-QF100SE-AD CS2245S YQPACK100SE CS2245T NQPACK100SE
H8S/2645,46,47,48	FP-144	CS2645A HY-2636/46-PB-QF128-AD CS2246B YQPACK144SD CS2246C NQPACK144SD
H8S/2643、43F H8S/2642、41	FP-144	CS2645K1 HY-2643-PB-FP144F-AD CS2246B YQPACK144SD CS2246C NQPACK144SD

* CPU package should be selected from the above list in order to choose the probe pod adapters on the debugging.
* CS2242E, Extension cable can not be used for H8S/2623 series, H8S/2636 series, and H8S/2646 series while Tokyo Eletec's extension cable can be used for H8S/2623 series and H8S/2646 series.
* The additional HQPACK(refer to the following) is required for CPU operation.

FP-128B - - - - - ---CS2245H HQPACK128RD FP-120 - - --- CS2245W HQPACK120SE
FP/TFP-100B - - - CS2231H HQPACK100SD FP-100A - - - CS2360W HQPACK100RB
TFP-100G - - - - - CS2245U HQPACK100SE FP-144G - - - CS2246H HQPACK144SD

Minimum Host System requirements for HyperSTAC/Watchpoint H8S/2633R Debugger*:*

OS: <USB>Windows98/Me/2000/XP <TCP/IP>Windows98/Me/NT/2000/XP
Memory: 32 MB (64 MB recommended)
Hard Disk: 20 MB

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