



The EP4080A is a single width, full height AMC processor board featuring the high performance Freescale QorIQ P4080 eight core PowerPC processor operating at up to 1.5GHz. The highly integrated multi-core processor makes the EP4080A a natural fit for combined control and data plane applications on a single board, thereby reducing system cost and power consumption. With broad operating support, the EP4080A is built for a broad range of demanding applications in wireless basestations, media gateways, enterprise network access systems, test and measurement systems, and server blades.

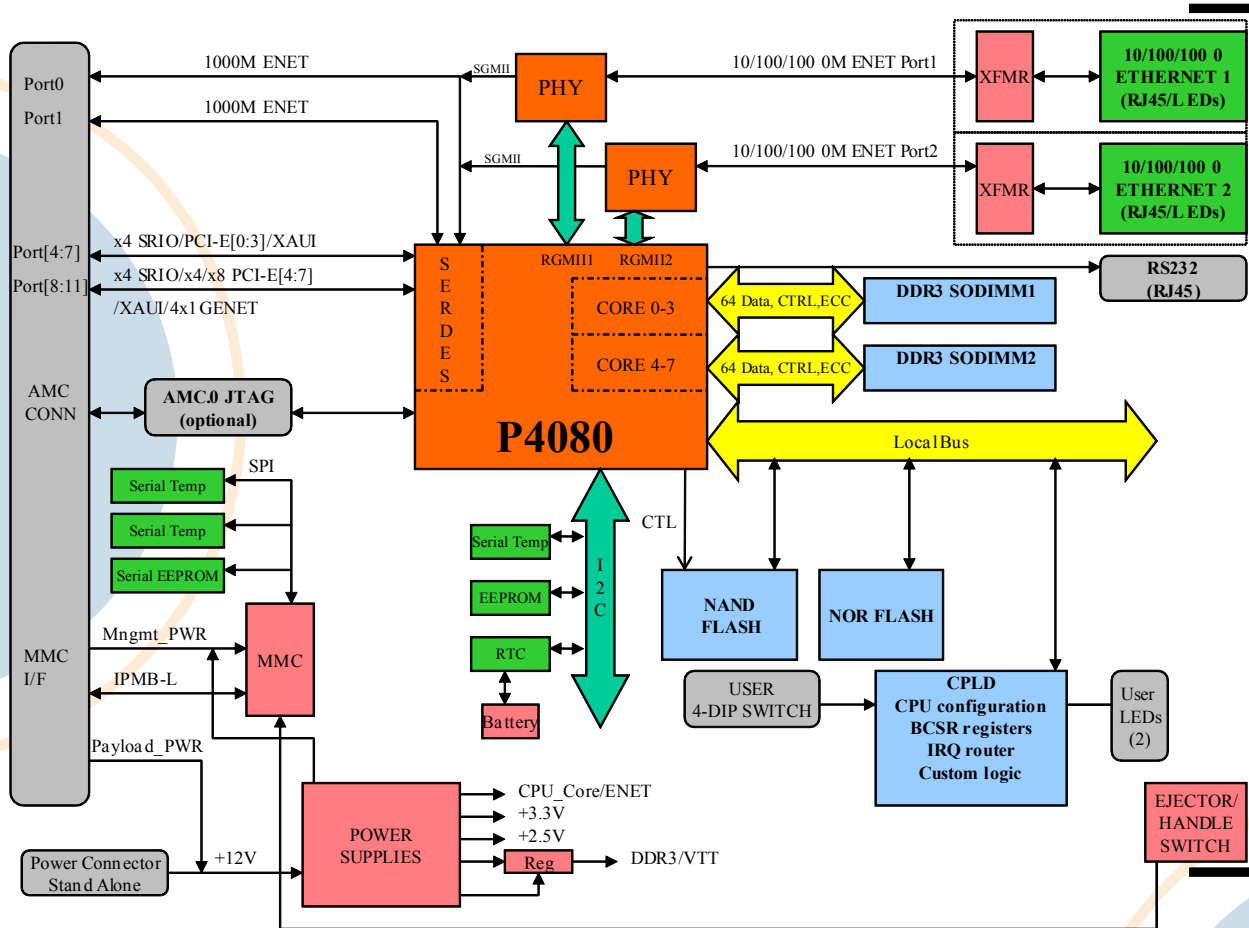
For fabric connectivity the EP4080A offers extreme flexibility, while maintaining standards compliance. All versions of the board support gigabit Ethernet on AMC channels 0 and 1, compliant with AMC.2, Type E2. The fat pipe region of the AMC (channels 4 - 11) can be configured on a build basis to support 10G Ethernet XAUI, Gen 2 PCI express, and SRIO.

Feature Summary:

Specification:	Description:
Form Factor:	Full or Mid-Height AMC.0
Backplane Options:	2 x GbE to AMC channels 0 and 1 with options for Serial RapidIO, Gen 2 PCI Express, and 10G Ethernet XAUI on the fat pipes. The fat pipes can be configured in combinations and be targeted for ports 4-7 or 8-11.
Front Panel:	2 x GbE connections and 1 x RS-232 serial
Processor:	Freescale Eight-Core QorIQ P4080 at up to 1.5GHz
Memory:	Up to 8 GB DDR3 with ECC in two SODIMMS, up to 128 MB of NOR flash and 1GB of NAND flash
Debug:	JTAG/COP via an onboard connector
Power Supply:	Via AMC connector per AMC.0 or from barrel connector
Software:	U-Boot bootloader, Linux, INTEGRITY, and VxWorks BSP available

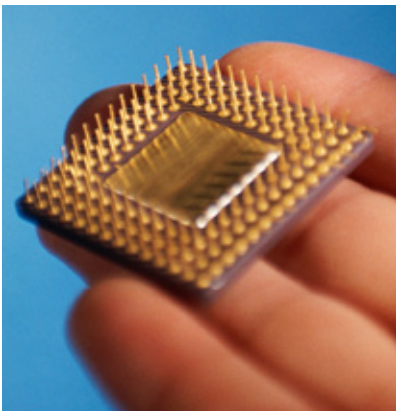
At the heart of the EP4080A is a Freescale QorIQ P4080 eight-core PowerPC processor. The P4080 is a highly integrated system-on-chip (SoC) platform that includes eight e500 PowerPC cores, an integrated security engine, integrated Gen 2 PCI Express, Serial RapidIO, Gigabit Ethernet, 10G Ethernet XAUI controllers, integrated DDR3 memory interface, and a pattern matching engine for packet inspection. The highly integrated SoC architecture improves system performance, increases system flexibility, lowers power consumption, and reduces overall system cost.

Hardware Block Diagram



A M C F R O N T P A N E L

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