

# CORELIS

- Connects up to four concurrent and independent ARINC-629 Channels at a time
- Intelligent VXI card with an on-board autonomous processor per channel
- Each channel can send/receive simultaneously at top speed
- Multiple Terminal Emulation capabilities, up to 120 Terminals per channel
- Extensive ARINC-629 bus error injection and detection capability
- Programmable Traffic Generator mode can transmit arbitrary ARINC-629 data, including user injected intentional errors
- On-board 4 MByte Shared Memory per channel
- Flexible Traffic Collection Buffering Accessible in Real-time and Supporting Endless Recording
- Enables a High-performance interface between a host PC and multiple ARINC-629 busses
- Pseudo Bus (TTL) or SIM Bus (via external CMC to ARINC-629 twisted-pair) interfaces supported - software selected
- LabWindows Demo Software Provided
- Host Software Driver Using Extensive LabWindows "C" DLL Library Calls and Utilities

## Applications

- Avionics LRU/SRU Qualification
  - Observe Bus Interactions
  - High Traffic Stress Test
  - Bus Access for Software Simulation
- System Integration
  - Live Environment Simulation
  - Characterize Performance
  - Bus Infrastructure Network Qualification
- Factory Acceptance Testing
  - Operational Validation
  - Test/Burn-in Cycling
- Field Support
  - Re-confirm Unit Behavior
  - Test Upgrades
  - Debug Failed Units
  - Debug Bus Network

## CVXI-629™ ARINC-629 Tester Card



## Overview

The CVXI-629 is a single slot "C" size VXI Revision 1.4 compatible module designed to provide broad ARINC-629 bus testing capabilities. This includes monitoring of ARINC-629 bus traffic, multiple terminal emulation, and fault insertion and detection.

Board versions available provide from one to four ARINC-629 channels resident on a single slot Multiple Device Module. Each channel consists of an independent VXIbus Message

Based device, utilizing a Boeing approved DATAC component for single terminal data transmission and reception. Standard bus modes supported include Periodic, Aperiodic, C, Block, Alternate, and Independent.

Up to 120 virtual terminals can be operated concurrently per channel run by its dedicated processor via embedded firmware. Additionally, an arbitrary freeform traffic generation format is also provided. This enables stressing of attached de-

vices using non-compliant formats.

Each of the independent channels can operate on its own ARINC-629 bus concurrently, attached via its dedicated front-panel connector. It can test, emulate, monitor and insert faults at the full data rates, continuously with a suite of external devices. The host PC sees each channel as a distinct VXI instrument.

The ARINC-629 test busses can be software selected to use the avionics SIM Bus signaling (with a user-provided external CMC attached to its terminated twisted pair), or the TTL open-drain Pseudo Bus. The latter supports software development without the need for the full suite of avionics bus interface hardware.

## Special Features

The CVXI-629 is a complete ARINC-629 Tester on a single slot VXIbus plug-in card. It is specially designed for testing and simulation of ARINC-629 communication interfaces and is an ideal solution for design engineers, manufacturing testers, simulation labs, and field maintenance facilities. The CVXI-629 incorporates many hardware and firmware features that make it both easy to use and yet highly programmable and flexible. The following is a list of some of the special features of this module:

- Full ARINC-629 bus monitoring capability, including features that are not available with the standard Boeing DATAC chip such as receiving all Label words including messages sent by the card itself.
- All received messages are time tagged with a 40-bit time stamp with 0.5  $\mu$ sec resolution. The user can record the data in memory (which the host can pipe to an external hard disk) in real time for later reconstruction or replay.

- The shared memory on-board is 4 Mbyte, enough to support the most demanding applications.
- Emulate up to 120 terminals on the 629 bus, each independently talking on the bus.
- Traffic generator mode is useful for creating arbitrary traffic that does not have to conform to the 629 bus specification and/or limitations. Use it to test the TI, TG and SG timers on your target system or to evaluate its response under extreme or faulty conditions.
- When emulating 120 terminals, the user can either provide an XPP for each terminal or can control the 629 bus bit stream directly via the Traffic generator mode.
- Intelligent card with on-board RISC CPU per channel can perform 629 communication tasks autonomously without host intervention freeing it up for other activity.
- Bit and word level error injection features are host programmable on a word-by-word basis. Message and protocol level errors can easily be created. The user can arbitrarily decide where and when to inject errors with many variations.
- The multiple concurrent channels simplifies connecting to several 629 buses as no external switching hardware is required.
- Both Pseudo Bus (Voltage mode) and SIM Bus (Current mode) 629 interfaces are implemented. Power to the external Current Mode Coupler (CMC) is provided by the CVXI-629 card. If supported by the UUT, the Pseudo Bus interface can be used to connect directly to the UUT avoiding the expensive CMCs.
- Input and output triggers are provided at the front panel connector of the card. This allows

synchronization of the operation of the CVXI-629 to external instruments.

- Several LabWindows demo programs are provided to quickly enable observable module behavior on the 629 bus. Some of these can also serve as user application development prototypes.

## General Description

The CVXI-629 is a VXI based ARINC-629 Bus Tester module that fits in a single slot of a "C" sized VXI chassis. It is designed to provide a wide range of features for testing and simulation applications of ARINC-629 compatible systems. The CVXI-629 is specially designed to support multiple terminal emulation, monitoring of ARINC-629 bus traffic and fault insertion and detection. The ability to emulate up to 120 ARINC-629 data terminals in the normal periodic fashion is provided as well as arbitrary traffic generation and error injection.

The terminal emulator can be programmed to generate user defined ARINC-629 bus traffic operating in any one of five modes as follows:

1. Single Terminal and bus monitor
2. Multiple Terminal Emulator (MTE)
3. Traffic Generator mode
4. Multiple Terminal Emulator with error injection
5. Traffic Generator with error injection

On-board Boeing approved Data Terminal (DATAC) devices are used for single terminal data transmission and reception. This is connected to Boeing approved SIM devices. The Transmit Personality PROM (XPP), Receive personality PROM (RPP) and Multiple personality PROM (MPP) for the DATAC chip are implemented using a host downloadable static RAM device rather than the traditional ROM.

A 128K x 8 SRAM chip provides four 8K byte XPP memories, one 32K byte RPP memory, and one 64K byte MPP memory for the ARINC-629 terminal. The memory content is similar to the standard 629 personality memories.

The Multiple Data Terminal Emulator, error injector and Traffic Generator logic is implemented with on-board field programmable gate array (FPGA) devices. The DATAC chip is bypassed by the logic so that the user has full control over the serial bit-stream that is sent to the 629 bus. The user is able to simulate irregular 629 bus traffic and insert intentional faulty conditions. The on-board firmware transfers the memory based transmit buffers to the front-end transmitter logic where it is converted into a 629 bus bit-stream.

The CVXI-629 card is ideal for test and simulation of faulty 629 bus conditions and the user can test the Unit Under Test (UUT) under ex-

treme or even illegal conditions. UUT features such as error recovery, exception handling and 629 bus gap timers default settings are readily testable.

## Multiple Terminal Emulator

The Multiple Terminal Emulator (MTE) is the most commonly used mode of the CVXI-629 card as it allows the user to create XPP-like transmit schedules for up to 120 terminals in the Shared Memory of the CVXI-629 device. Using these transmit schedules, the CVXI-629 generates bus traffic to represent these terminals as if they were individually transmitting on the 629 bus. The card continues to monitor and

store incoming traffic while this behavior is underway. This behavior can be programmed as required for each channel.

The MTE mode of operation is somewhat similar to the Traffic Generator Mode of operation, except in the manner that the terminals are represented in the Shared Memory of the CVXI-629. The MTE mode offers the following advantages over other modes of operation:

1. Since CVXI-629 (transmitter) operation is no longer tied to a single XPP, the module has the ability to emulate multiple terminals on the 629 bus. By loading the appropriate data, the user can emulate any number of 629

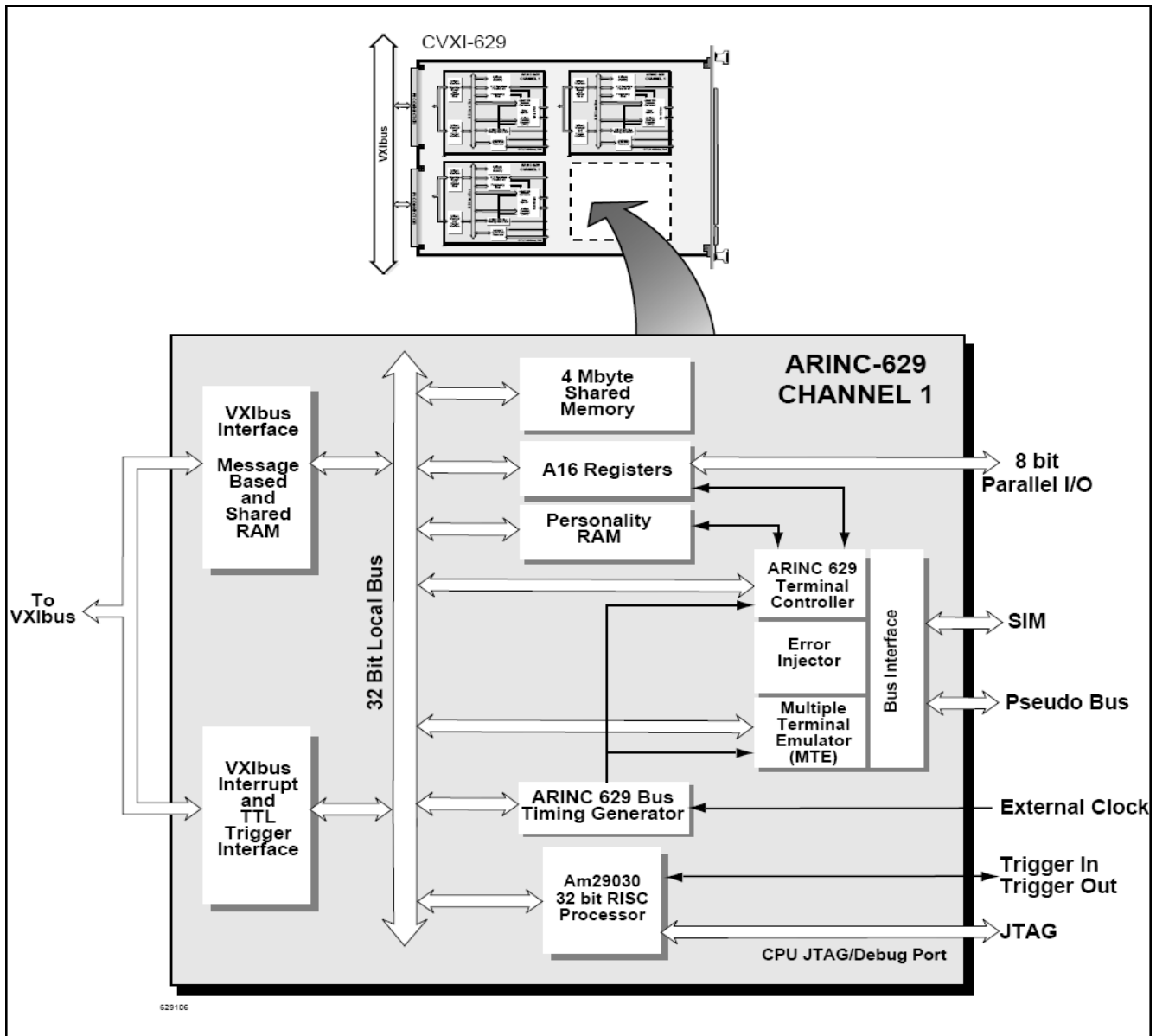


Figure 1. Block Diagram

terminals (up to the maximum of 120). This allows the user to simulate 629 bus loading and system characteristics using only a single PCI plug-in card.

2. The terminal scheduling information is represented in an XPP-like format memory structures, making it simpler to specify Block or Independent scheduling than the Traffic Generator Mode.

Errors can be injected at all levels (word-by-word, wordstring, and message). When using a Standard Terminal Controller (DATAc) chip, the types of errors that can be generated are very limited. By providing this mode of operation, in addition to Single Terminal Mode and Traffic Generator Mode, a broad spectrum of testing situations is supported.

This mode also supports the generation of CRC information. A refresh counter mechanism is also available to automatically advance data values.

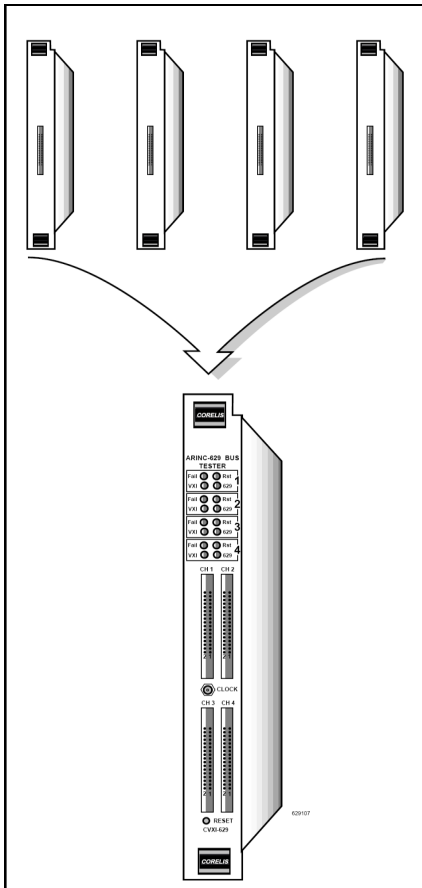


Figure 2. "4-in-1" module concept

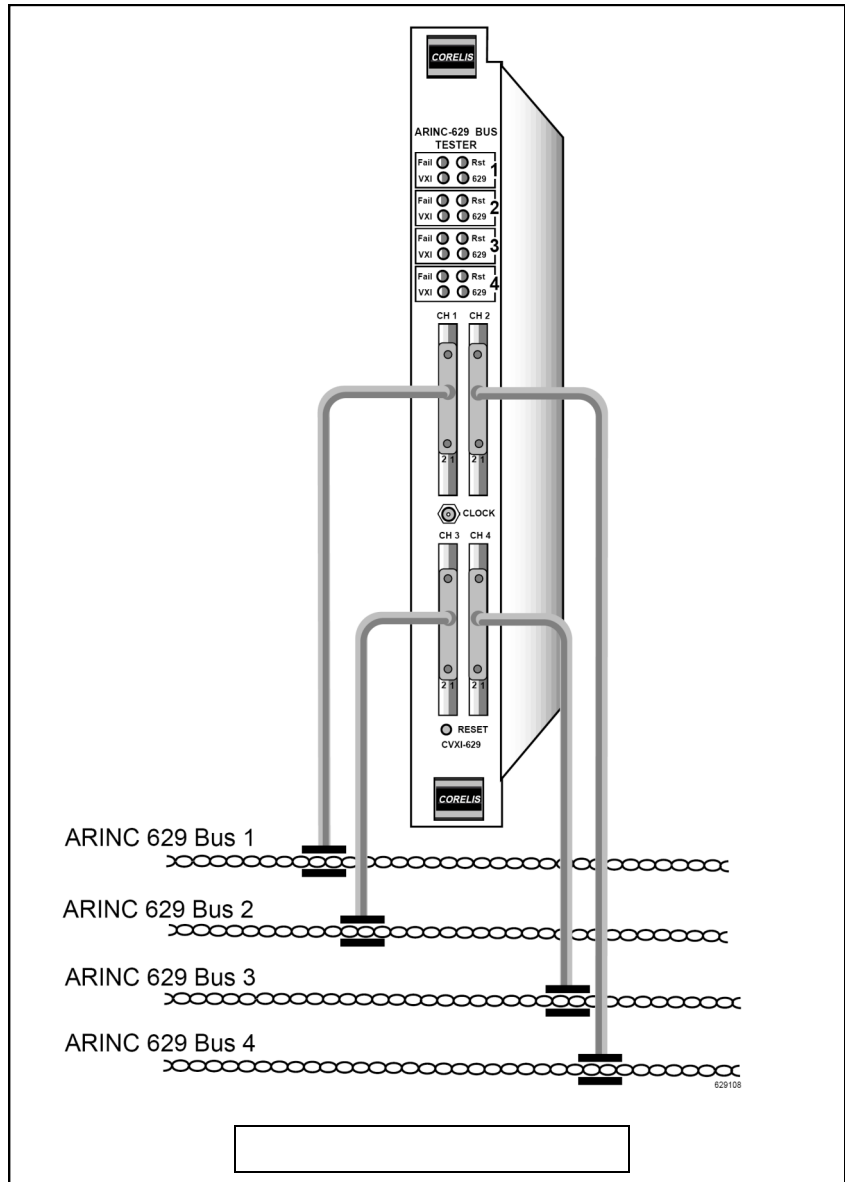


Figure 3. Multiple Bus connectivity

### 629 Bus Traffic Generator

This feature is very similar to the MTE mode except it enables free-form, non-scheduled emulation of up to 120 terminals. The user sets up transmit information whose structure is unconstrained by the ARINC-629 timing scheme and other limitations. This enables creating traffic of a more arbitrary nature to stress devices on the bus. See Figure 4 for a block diagram.

### CVXI-629 Architecture

The CVXI-629 contains the following hardware functional blocks per channel:

- VXIbus Interface
- 4M byte shared memory
- On-board CPU
- Transmit (TX) FIFO memory
- Receive (RX) FIFO memory
- Traffic Generator logic
- Terminal Controller (DATAc) device
- Serial 629 bus Interface Module (SIM).

When the CVXI-629 is in the MTE mode of operation, the transmitter of

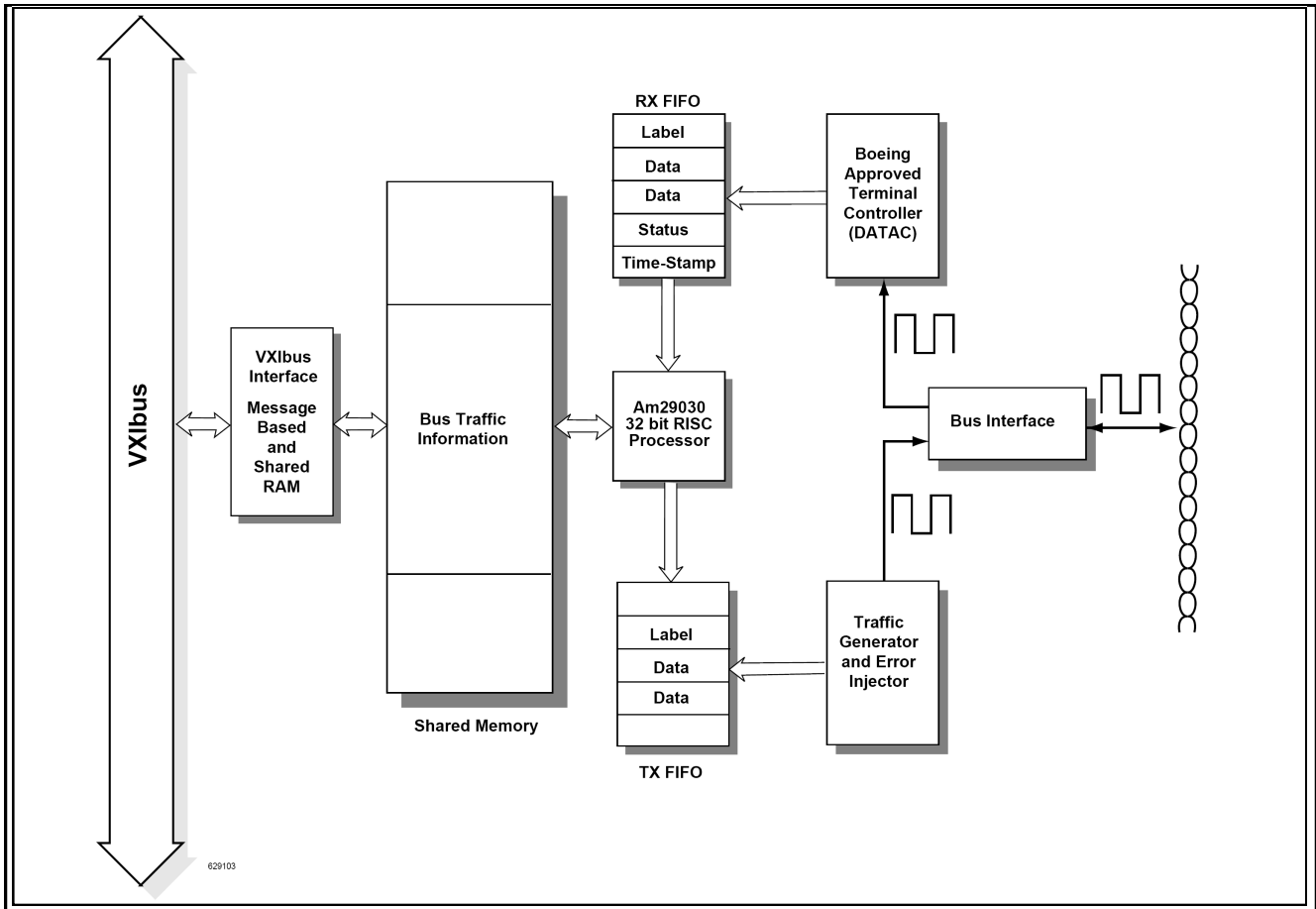


Figure 4. Arbitrary Bus Traffic Generator

the on-board DATAC is switched out of operation and a highly programmable, specially developed Traffic Generator is switched into its place. The shared memory, which can be accessed by the host PC via the VXI interface and by the CVXI-629 internal CPU, provides a global data storage resource. Information required for this mode of operation is stored in the shared memory by the user.

The CPU takes the information stored by the user and converts it into the format required for the Traffic Generator. The Traffic Generator communicates with the onboard CPU via the TX FIFO memory which was used in order to utilize the maximum throughput of the CPU. Loading of the data by the CPU into the TX FIFO memory is asynchronous to the activity of the 629 interface (DATAC and/or Traffic Generator), freeing the CPU to serve other functions as well, such as PC host communication.

The Traffic Generator reads information written to the TX FIFO by the CPU and uses the timing, control, and data content and converts it to waveforms required for bus operation. The Traffic Generator, besides its normal transmit function, allows the injection of a wide variety of errors into the normal bus traffic.

### Shared Memory

All ARINC-629 data is sent from and received into an on-board three-port shared memory. Up to 4 Mbytes of memory can be allocated to the transmit data and the multiple received data buffers. The memory is accessible to the onboard 29030, the DATAC chip transmitter logic, and to the host computer. Arbitration of the shared memory is transparent to all parties. The user can program multiple wordstring buffers (default is double buffered). No host overhead is required to maintain the multiple receive buffers, although it will need to extract in background for endless data collection.

### Bus Monitor Receiver

Received messages are logged into a circular queue buffer on a First In First Out (FIFO) structure in shared memory. The user can program the card to either receive all of the 629 bus messages, including label words, or to screen the incoming messages for wordstrings of interest.

All wordstrings received are stored in the FIFO along with time-stamp and status information. The FIFO memory size is user programmable (default is 64K byte). All incoming messages are time-tagged and then stored into this FIFO memory in addition to being stored in an alternate shared memory buffer grouped by Label.

The time tag is a 40-bit time word with 0.5  $\mu$ sec resolution. The time tag counter can be reset via a host

command or by an external trigger via the front panel connector.

## Data Terminal IC Settings

The Boeing compliant DATAC chip is used in the single terminal mode to transmit and receive data over the ARINC-629 bus. It has programmable pins that are under software control enabling the user to configure the desired settings.

The Transmit Interval (TI), the Synchronization Gap (SG) and the Terminal Gap (TG) are user programmable by commands to the module. The commanded values are directly connected to the corresponding input pins of the DATAC chip. The user is able to program a 7-bit value for the TG, a 7-bit value for the TI and a 2-bit value for the SG.

The user programmable channel ID (CID) enables identical labels to be transmitted by different terminals. Identification of the label's source is accomplished by inserting a unique channel ID (CID) in front of each label. The CID bits are programmed by command to the module. The user may elect to dynamically change the CID bits for each message by programming the AXT field (4-bits) in the XPP to one of the 16 possible values. This feature allows simulation of multiple terminals using a single terminal. Switching the source of Channel ID is done through a command to the module. By utilizing the CID control, the EXT field of the label words may be dynamically changed on the fly.

## Error Injection

The Multiple Terminal Emulator (MTE) can be programmed to inject predefined errors during data transmission. Error tag bits are appended to each data word in memory supporting errors on a word-by-word basis. Word/Bit level errors are generated by dedicated hardware and are injected each word depending on the tag bits. There are a few errors that the user can program at the protocol level such as a Short String Error, an Impersonation Error, etc. The following errors can be generated:

### Parity Error

Inverted (Even) parity bit is sent to

the 629 bus on a word-by-word basis.

### Inverted Sync Error

The 3 Sync bits of any word can be inverted on a word-by-word basis.

### Sync Bit Error

The 3 Sync bits can be distorted with a Manchester Bi-Phase type error on a word-by-word basis.

### Manchester Error

Illegal Manchester Bi-Phase bits are inserted anywhere in the 20-bit Manchester word format (including Sync and Parity bits). The Manchester error can be programmed in 1/4 bit resolution to any combination of high, low and mid (gap) levels for each of the four 1/4 bit slices. Can be programmed on a word-by-word basis.

### Short Word Error

A bit is replaced with a single-bit gap at the tail end of the word on a word-by-word basis.

### Long Word Error

An additional bit is appended to the last bit of the last word of a word-string.

### Bus Contention Error

An ARINC-629 bus contention is generated by enabling the SIM to send a word whenever another terminal is transmitting. This is comprised of one Manchester bit, creating a one-bit data contention.

### Impersonation Error

The XPP can be programmed to send the same CID bits as another transmitter, causing an impersonation error. This does not require any hardware intervention being supported by the downloadable personality PROM of the CVXI-629 card.

### Short String Error

The XPP can be programmed to send fewer words in the wordstring than is expected by the UUT. This error does not require any hardware intervention being supported by the downloadable personality PROM of the CVXI-629 card.

### End-of-String Error

The XPP can be programmed to send more words than is expected by the UUT for the particular wordstring. This error does not require any hardware intervention being sup-

ported by the downloadable XPP of the CVXI-629 card.

### Frequency Error

The clock source for the CVXI-629 can be selected from one of four possible data rates: 32 MHz (nominal), 30 MHz (low), 33 MHz (high) or External Clock input from the front panel connector. This supports stressing the receive timing of terminals on the bus.

## Receiver Errors Detection

The ARINC-629 receiver circuitry is capable of detecting both protocol and format (hardware) type errors. This is performed by the DATAC chip and by post-processing of the received messages by the on-board microprocessor. The following errors can be detected:

### Parity Error

Inverted (Even) parity bit is received from the 629 bus.

### Impersonation Error

The received label's extension does not agree with the terminal's CID when the MSC field in the appropriate RPP cell is not equal to 1F hex.

### Short String Error

The received wordstring was shorter than expected and it terminated prematurely.

### RERF Error

This indicates that the DATAC chip encountered a data integrity error, possibly an improper Manchester code, SYNC or parity bit error.

### PAM0 Error

This indicates a disagreement between the RPP content and the TG or SG register.

### PAM1 Error

This indicates a disagreement between the RPP content and the TI register.

## Bus-Monitor Error Detection

The DATAC chip contains a built-in bus monitor that can detect errors associated with the reception of data that is being transmitted by the terminal itself. The following errors can be detected:

### End of String Error

The received wordstring contains more words than are expected by the UUT.

### End of Message Error

The number of actual wordstrings exceeds the Message String Count (MSC) field of the RPP.

### Data Error

A Manchester encoding error, parity or Sync error.

### Label Error

A label word Manchester encoding error, parity or Sync error.

### XERF Error

This indicates detection of a data integrity error, which prevented transmission. This error is flagged by the DATAC internal Error register.

### TXE

Indicates that the transmitter was permanently shut off due to detection of multiple (7) errors. To re-enable the transmitter of the DATAC, the chip must be reset. Note applies only in a single terminal mode where the DATAC transmitter is enabled.

### Bus Quiet Error

One or more transmit word is missing, thereby creating an unexpected bus quiet state.

## ARINC-629 Bus Rate

The ARINC-629 bus clock source is programmable: on-board 32 MHz XTAL oscillator (nominal), on-board 30 MHz XTAL oscillator (slow), on-board 33 MHz XTAL oscillator (fast), external clock source via the front panel connector. The selected clock source can optionally be divided by two to provide ARINC-629 protocol compatible operation, but running at MIL-STD-1553 data rates (1M baud nominal).

## VXIBus Interface

The CVXI-629 module is a single slot "C" size module. Each channel interfaces with the VXIBus as an A16/A24/A32 D16/D32 Message Based slave compatible with VXIBus 1.4, containing shared RAM.

The VXIBus Interrupt Requester (Interrupter) priority level is user programmable.

Bus options, including addressing, are DIP switch selectable.

Each channel of the CVXI-629 is a stand-alone instrument as seen by the host. Typically, the user supplies a PC host as a VXI resident processor/slot-0 controller, or as an external PC connected via a slot-0 controller using a MXI link.

## LEDs

The front panel LEDs are located at the upper portion of the front panel. There are four LED indicators for each 629 channel:

The **Rst** red LED indicates that the on-board CPU for the particular channel is reset by the host.

The **Fail** red LED is lit upon power-up when the CPU executes its self test. If lit for more than 5 seconds, it indicates a selftest failure.

The **VXI** green LED indicates that the device is being accessed by the VXIBus host.

The **629** green LED is lit every time that the device is transmitting data over the 629 bus.

## Reset Switch

A push-button momentary switch on the card can be used to reset the card, including all channels, in a similar mode to a power-up reset.

## SIM/CMC Power

+/- 15V power for the SIM and CMC are provided by an on-board DC-DC converter. The user can also configure the card to receive input power for the SIM and CMC from the front panel connector.

## Connection to Multiple 629 Busses

A number of Units Under Test (UUTs) contain more than one ARINC 629 interface. The CVXI-629 can simplify the testing of these UUTs operating up to 4 separate ARINC 629 busses independently and concurrently. The 4 sets of transmit/receive (both Pseudo Bus and SIM Bus) signal pairs are avail-

able at the front panel connector of the card, per channel. The SIM Bus ports require an external CMC each.

For the Pseudo Bus, the on-board circuitry is used to switch the transmitter and receiver to the individual signal pairs logically. High-current, open-collector drivers are used for each of the Pseudo Bus signal pairs. Two 60 ohm termination resistors are also provided at the front panel connector for each Pseudo Bus signal pair. Note that these signals may be toggling when the SIM Bus is selected as active.

## Front Panel Connector

The front panel of the CVXI-629 contains four ARINC-629 interface connectors, one connector for each 629 channel. These connectors are labeled CH1-CH4. Each of the 629 interface connectors is functionally equivalent. These connectors provide the interface for the 629 bus coupler, pseudo bus, external triggers, external bus synchronization signals, and the JTAG bus.

The connectors are 34-pin 3M type header connectors that consist of two rows of 17 pins, spaced 0.1" apart. The pinout of the 629 interface connector is shown as Table 1.

Table 2 shows part numbers for 3M and AMP connectors which mate with the 629 interface connector.

Figure 6 shows the 629 interface connector as viewed when looking directly into the front panel of the CVXI-629.

## Host Software

Application software is provided to assist the user to quickly set up and observe card behavior. The CVXI-629 Device Utility is a graphical user interface (GUI) that provides an easy way to transmit, receive, monitor and in general exercise the functionality of CVXI-629 card. For users who prefer the most flexibility, custom "C" application software can be written using the CVXI-629 Instrument Driver. Included here are functions which mimic some of the more advanced behavior as found in the Tektronix ARINC-629 Analyzer.

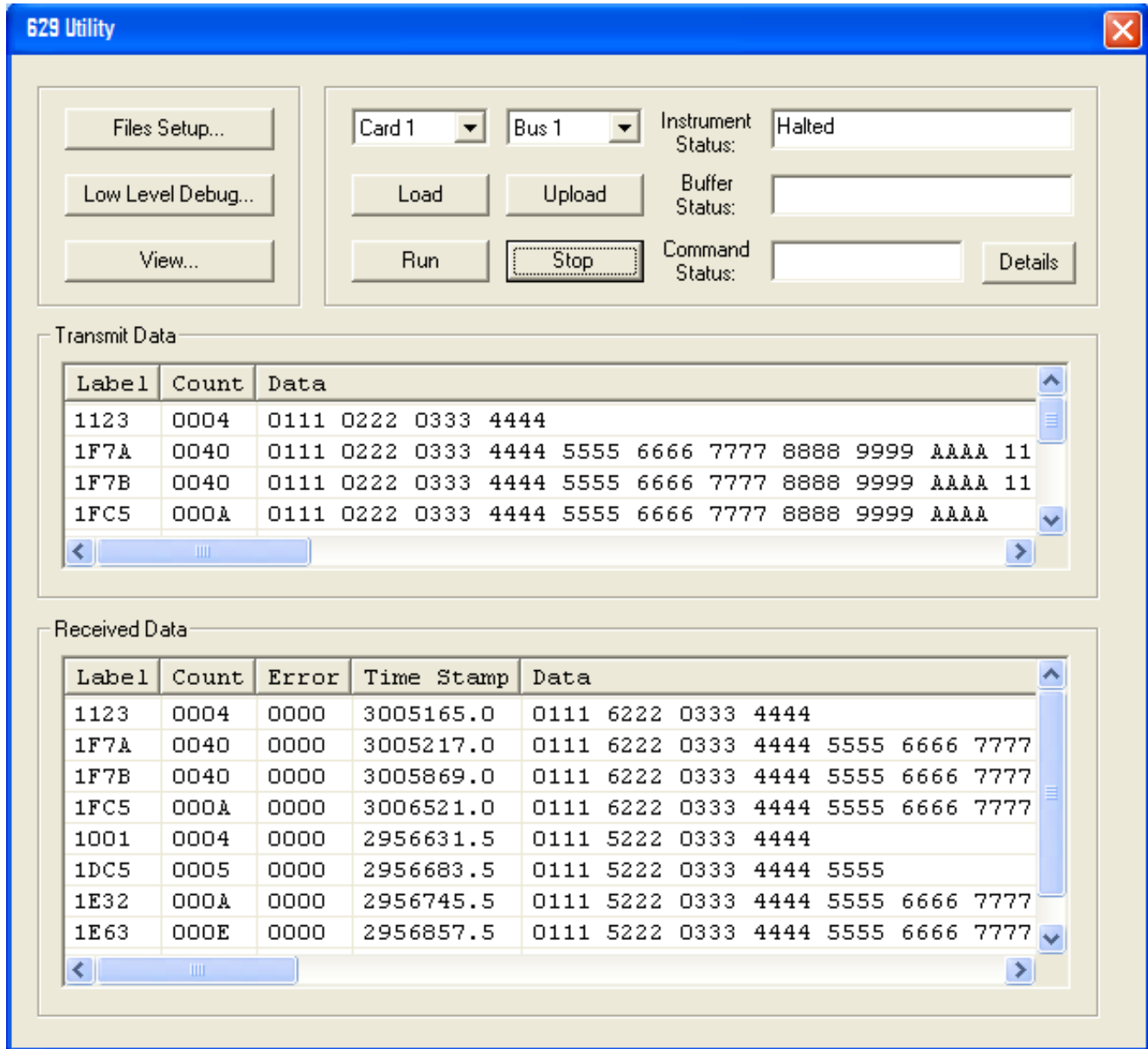


Figure 5. Utility Main Screen

Several LabWindows demo programs are provided to quickly enable observable module behavior. Some of these can also serve as user application development prototypes.

One Utility tool operates the card with text file controlled traffic simulation via friendly GUI screens. It can operate one or two channels, enabling loopback between them. See Figure 5 for an image of its top level screen.

Another provides a simple console demo program including source code. This shows calls to the in-

cluded DLL driver functions. It operates two channels, one looping to the other, listening to the traffic.

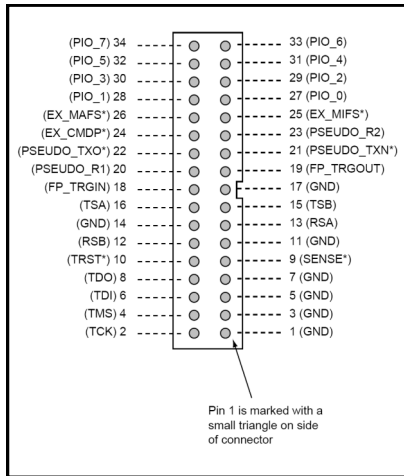
Finally, a more complex demo routine with source code operates the board with emphasis on the more advanced Tektronix-like features. Here, loopback between two channels is employed.

All demo software and drivers presume a LabWindows host running on a stand-alone PC linked with the VXI chassis via MXI.

Note: Familiarity with the ARINC-629 specification and with the 629

Avionics bus DATAC, SIM and CMC components is required in order to use this card and in order to write host application software that utilizes this card.

CVXI-629 Instrument Driver DLL software provides the capability to access all CVXI-629 functionality. Users who desire to write their own software will find this low level "C" driver software very useful. These functions make it easier to write custom application software and drastically reduce the software development effort.



**Figure 6.** 629 Connector

Pin	Signal Name	I/O	Description
1	GND	-	System Ground
2	TCK	In	JTAG TCK (factory use only)
3	GND	-	System Ground
4	TMS	In	JTAG TMS (factory use only)
5	GND	-	System Ground
6	TDI	Out	JTAG TDI (factory use only)
7	GND	-	System Ground
8	TDO	In	JTAG TDO (factory use only)
9	SENSE*	In	Target Cable Connected Sense
10	TRST*	In	JTAG TRST (factory use only)
11	GND	-	System Ground
12	RSB	In	ARINC 629 Bus Coupler Receive, B
13	RSA	In	ARINC 629 Bus Coupler Receive, A
14	GND	-	System Ground
15	TSB	Out	ARINC 629 Bus Coupler Transmit, B
16	TSA	Out	ARINC 629 Bus Coupler Transmit, A
17	GND	-	System Ground
18	FP_TRGIN	In	External Trigger Input
19	FP_TRGOUT	Out	External Trigger Output
20	PSEUDO_R1	-	60 Ω pullup to +5v
21	PSEUDO_TXN*	I/O	Pseudo Bus - Line 2 (open collector)
22	PSEUDO_TXO*	I/O	Pseudo Bus - Line 1 (open collector)
23	PSEUDO_R2	-	60 Ω pullup to +5v
24	EX_CMDP*	In	C-mode Pulse Input
25	EX_MIFS*	In	C-mode Minor Frame Sync
26	EX_MAFS*	In	C-mode Major Frame Sync
27	PIO_0	I/O	Parallel I/O 0 (LSB)
28	PIO_1	I/O	Parallel I/O 1
29	PIO_2	I/O	Parallel I/O 2
30	PIO_3	I/O	Parallel I/O 3
31	PIO_4	I/O	Parallel I/O 4
32	PIO_5	I/O	Parallel I/O 5
33	PIO_6	I/O	Parallel I/O 6
34	PIO_7	I/O	Parallel I/O 7 (MSB)

**Table 1.** 629 Interface Connector pinout

Manufacturer	Part Number	Type
3M	3414-6634	.100" x .100" Wiremount Socket
AMP	746285-8 or 746288-8	Novo Receptacles, Center and Military Polarized, .100 x .100 Centers

**Table 2.** Connector part numbers

## SHORT FORM SPECIFICATIONS

### VXibus Interface

Device Type	Message Based with shared memory interface
Protocol	Word Serial Protocol
Mode	A16/A24/A32,D16/D32 VXI Slave
Address Bus Width	24 or 32-bit for shared memory,16 bit for A16 registers
Data Bus Width	16 or 32-bit for shared memory,16-bit for A16 registers
Interrupter	Software programmable, IRQ1* to IRQ7*

### Shared Data Memory

Total Memory	16M Byte, optional 64M Byte
Per 629 Channel	4M Byte, optional 16M Byte.
Dual-Port	Host and local CPU accessible with transparent arbitration.
Data Width	16 or 32-bit

### Personality PROMs

XPP Memory	Four XPP memories, 8K Byte each, 32K Byte total. Host downloadable.
RPP Memory	Host downloadable 32K Byte RPP memory.
MPP Memory	Host downloadable 64K Byte MPP memory.

### ARINC-629 Interface

Data Terminal IC	Four XD1516 (or equivalent) ICs (one per channel)
SIM	Four AMP (or equivalent) ICs (one per channel)
Modes of Operation	Periodic (A-Mode), Aperiodic (BMode), C-Mode
Scheduling	Block, Independent, Alternate, Synchronized
Primary Speeds	2MHz (nominal), 1MHz (1553B compatible)
Near Nominal Speeds	103%, 94%, External

### Receive Queue

Continuous Buffer	Circular buffer type, 512K byte, shared memory based
Label Queue Buffer	Labels buffer records bus events. Size is 256K byte
One-Shot Buffer	Armed by trigger, then receives until full. Size is 256 Kbyte
Format	Complete wordstrings stored, each includes time-stamp and status words
Time Stamp Words	40-Bit time-stamp, 0.5 $\mu$ s resolution
Status Word	16-Bits status with error bits

### ARINC-629 Bus Monitor

Data Format	Each wordstring is received in full: Label Word, Data Word(s), Time Stamp, Status.
Label Filter	Receives all or filtered bus messages

### Error Insertion

Method	Error code tag for each transmit word.
Number of Errors	One per word, unlimited number of words, any time, any word(s),any message(s)
Error Types	Parity error Manchester error (1/4 bit resolution) Inverted sync error Sync error Short word error Bus quiet error Pre-sync pulse error Pre-pre-sync pulse error Inter-wordstring short gap error Inter-wordstring long gap error
Error Injection Order	User specified arbitrary order
Frequency Error	Clock source programmable: 32MHz (nominal), 33MHz, 30MHz, External (user supplied)

# SHORT FORM SPECIFICATIONS

## Multiple Terminal Emulator

Number of Terminals	Programmable to 120 terminals
629 Modes	Both Periodic and Aperiodic
Transmit Schedule	User Specifies up to 120 XPPs in shared memory
Transmit Order	User specified terminal order
Error Injection	Word by Word basis, any word
Error Detection	Status bits for each Word-string

## ARINC-629 Bus Coupling

Type	Both Current and Voltage
Current Coupler	SIMs with user provided (external) CMC interface
Voltage Coupler	Open Collector Pseudo-Bus Interface, 190 mA current sink
Termination	Two 59 ohm pull-up resistors per channel are optional

## DIP Switch Settings

A24/A32 Switch	A24 or A32 modes selection
Logical Address Switch	VXI Logical Address for channel 1. All remaining channels have consecutive logical addresses.
Address Inc Switch	Selects the VXI Logical Address increment for each device: +1 or +8

## Triggers

VXIbus TTLTRG*	One of eight triggers out, One of eight triggers in
Front Panel	One Trigger_In, One Trigger_Out for each 629 channel
Trigger Output Timing	User selectable, any word-string, leading or trailing the wordstring

## Physical Characteristics

Size	Single slot, "C" size
Dimensions	Approx. 13.4"L x 9.2"W x 1.2"D
Connectors	Four 34-pin 3M type connectors, one per 629 channel. One SMB connector for external clock input
LEDs	Four per channel: Rst (red), Fail (red), VXI (green), 629 (green)

## Configurations

The module is available in multiple configurations to meet the particular customer requirements. Either one (CVXI-629/1), two (CVXI-29/2), three (CVXI-629/3) or four (CVXI-629/4) channel configuration can be ordered, with or without the SIM module(s) and with or without expanded shared memory. Table 3 shows the various available configurations.

Model	629 Channels	SIM Modules	Shared Memory
CVXI-629/4-S	4	4	16M Byte
CVXI-629/3-S	3	3	12MByte
CVXI-629/2-S	2	2	8M Byte
CVXI-629/1-S	1	1	4M Byte

Table 3. CVXI-629 Configurations

## Ordering Information

Part Number	<b>CVXI-629/n-S</b> n = No. of channels (1,2,3 or 4) S = SIM installed, all channels
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